Call for Papers

International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
September 29 – October 04, 2024, *Raleigh, NC, USA*

The International Conference on Hardware/Software Codesign and System Synthesis (**CODES+ISSS**) is the premier conference in system-level design, hardware/software co-design, modeling, analysis, and implementation of modern embedded systems, cyber-physical systems, and internet-of-things, from system-level specification and optimization to synthesis of system-on-chip hardware/software implementations. CODES+ISSS is part of Embedded Systems Week (ESWEEK), the premier event covering all aspects of hardware and software design for smart, intelligent, and connected computing systems.

Journal Track Submissions:
Abstract Submission: March 24, 2024
Full Paper Submission: March 31, 2024 (firm)
Acceptance Notification: July 14, 2024

Late Breaking and Work-in-Progress Tracks:
Full Paper Submission: June 02, 2024 (firm)
Acceptance Notification: June 30, 2024

All submissions are due by midnight, AOE.

We invite submissions on **all aspects of embedded systems design**, including but not limited to:

Track 1 [System-level design]: Specification, modelling, refinement, synthesis, and partitioning of embedded systems, hardware-software co-design, hybrid system modeling and design, model-based design, design for adaptivity and reconfigurability.

Track 2 [Domain/application-specific design]: Analysis, design, and optimization techniques for multimedia, medical, automotive, cyber-physical, IoT, and other application domains.

Track 3 [System architecture]: Heterogeneous systems, many-cores, and distributed systems, architecture and micro-architecture design, exploration and optimizations of application-specific processors and accelerators, reconfigurable and self-adaptive architectures, storage, memory systems, and networks-on-chip architectures.

Track 4 [Simulation, test, validation, and verification]: Hardware/software co-simulation, test generation, verification and validation methodologies, formal verification, assertion-based validation, hardware acceleration, simulation and verification languages, models, metrics, and benchmarks.

Track 5 [Embedded software]: Language and library support, compilers, runtimes, parallelization, software verification, memory management, virtual machines, operating systems, real-time support, middleware.

Track 6 [Safety, security, and reliability]: Cross-layer reliability, resiliency and fault tolerance, test methodology, design for security, reliability, and testability, hardware security, security for embedded, CPS, and IoT devices.

Track 7 [Power-aware systems]: Power-aware and energy-aware system design and methodologies, ranging from low-power embedded and cyber-physical systems, IoT devices, to energy-efficient large-scale systems such as cloud datacenters, green computing, and smart grids.

Track 8 [Embedded machine learning] Hardware and software design, implementation, and optimization for machine learning that are specially designed for resource- and power-constrained embedded, CPS, and IoT devices.

Track 9 [Industrial practices and case studies] Practical impact on current and/or future industries, application of state-of-the-art methodologies in areas including wireless, networking, multimedia, automotive, IoT, etc.

Submitted manuscripts will go through **double-blind** review. Authors should not reveal their identity directly or indirectly (e.g., through references). The submitted work must be **original**, not formerly published or under review elsewhere.

Journal-Integrated Publication Model: All full papers accepted in CODES+ISSS 2024 will be published in the **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)**. All late-breaking papers accepted in CODES+ISSS 2024 will be published in the **IEEE Embedded Systems Letters (ESL)**. See details at https://esweek.org/author-information

ESWEEK General Chairs:
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