



Embedded Systems Week

www.esweek.org

September 29 – October 4, 2024
Raleigh, NC, USA

CASES 2024

CASES

Call for Papers

**International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
September 29 – October 4, 2024, Raleigh, NC, USA**

CASES is a premier forum, where researchers, developers, and practitioners exchange information on the latest advances in design, optimization, validation, and applications of embedded systems, Internet of Things (IoT), and the emergent trend of integrating Artificial Intelligence into IoT (AIoT). The conference has a long tradition of showcasing cutting-edge research in these broad areas, covering topics including, but not limited to, hardware-software co-design and co-validation, edge AI, embedded architecture, compilers for heterogeneous systems, memory/storage technology, security/reliability, energy-efficiency of embedded systems, and domain-specific hardware accelerators. We solicit submission of original research articles on these topics divided into five technical tracks. Each submission needs to specify one primary and one secondary track relevant to the paper's technical content.

TRACK 1: AI Systems and Applications of AI at Edge

Artificial Intelligence of Things (AIoT), Edge intelligence, Architectures, accelerators, and compilers for AI hardware; Applications of machine learning techniques to embedded systems, IoT, and Cyber-Physical Systems (CPS); Neuromorphic and cognitive computing, analytics for embedded applications; and validation techniques for AI components.

TRACK 2: Embedded Systems and IoT/CPS Security, Safety, Reliability, and Energy-Efficiency

Secure architectures, hardware security, software security for embedded systems, IoT, and CPS; Architecture, design, and compiler techniques for energy-efficiency, reliability, and aging; Modeling, analysis, and optimization for timing and predictability; Validation, verification, testing, and debugging of embedded software.

TRACK 3: Memory and Storage

Memory system architecture; Persistent memory, Emerging memory technologies (e.g., ReRAM, MRAM, FeRAM, DNA); Caches, scratchpad memory, and compiler-controlled memory; Reconfigurable memory; and storage systems.

TRACK 4: Accelerators, Emerging Technologies, and Applications

Synthesis, optimization, and design-space exploration of high-performance, low-power, reliable accelerators; Domain-specific accelerators for emerging applications including AI training/inference, graph analytics, scientific computing; Compilers for accelerators; Biologically-inspired computing; Heterogeneous and domain-specific multi-core SoC; Approximate computing; Flexible hybrid electronics (FHE); Augmented/virtual reality.

TRACK 5: Architectures, Compilers, System-level Design

Embedded and mobile processor micro-architecture, Many-core processors, GPU architectures, Reconfigurable computing including FPGAs and CGRAs for embedded systems and IoT/CPS, Application-specific processor design, 3D-stacked architectures; Networks-on-Chip (NoC) architectures; I/O management in embedded systems; and compiler support for CPU, GPU, reconfigurable computing, emerging computing paradigms, compilation for memory, storage, and on-chip communications.

Journal Track:

Abstract Submission: March 24, 2024

Full Paper Submission: March 31, 2024 (firm)

Notification of Acceptance: July 14, 2024

Late Breaking and Work-in-Progress Tracks:

Paper Submission: June 2, 2024 (firm)

Notification of Acceptance: June 30, 2024

Proposals of Workshops, Tutorials, Education Classes, and Special Sessions: March 24, 2024

All submissions are due by midnight, AOE.

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Journal-Integrated Publication Model: Journal-Integrated Publication Model: All full papers accepted in CASES'24 will be published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). All late-breaking papers accepted in one of the three conferences will be published in IEEE Embedded Systems Letters (ESL). See details at <http://www.esweek.org/author-information>

ESWEEK General Chairs:

Alain Girault, INRIA, France

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