

All times are Eastern Daylight Time (EDT).					
Friday, September 27					
	Virtual	Virtual	Virtual	Virtual	
10:00-12:00	Education class 1. Design Space Exploration for Deep Learning at the Edge. Authors: A.D. Pimentel.	Education class 2. Enabling Energy-efficient AI Computing: Leveraging Application-specific Approximations. Authors: S. Ullah.	Education class 3. Efficient Neural Networks: from SW optimization to specialized HW accelerators. Authors: M. Traiola.	Education Class 4. Primer on Data on Quantum Machine Learning Authors: A. Shrivastava.	
16:00-18:00	Education class 5. AI-Driven Indoor Navigation with Mobile Embedded Systems. Authors: S. Pasricha.	Education class 6. MLSysBook.AI: Principles and Practices of Engineering Artificially Intelligent Systems Authors: V.J. Reddi.	Education Class 7. Spiking Neural Networks and MatMul-Free LLMs Authors: J. Eshraghian.		
Sunday, September 29					
	Hannover I	Hannover II	Hannover III	Governor I	Governor II
09:00 - 10:30	Tutorial 1. Disruptive Memory Technologies: A Tutorial and Unified Simulation Framework. Authors: J.-J. Chen (TU Dortmund), J. Henkel (KIT), L. Siddhu (KIT).	Tutorial 2. Low Code, High Performance Embedded AI with MATLAB & Arm IP Explorer. Authors: B. Zhuang (MathWorks), A. Rajhans (MathWorks), E. Sondhi (Arm).	Tutorial 3. AMD's Ryzen AI Neural Processing Unit Hands-on Tutorial. Author: A. Schmidt (AMD).	Tutorial 4. Privacy Preserving Primitive for Health Data. Authors: F. Regazzoni (University of Amsterdam), P. Palmieri (University College Cork), A.P. Fournaris (ISI).	Tutorial 5. ARES: AI for Science on Resource-Constrained Embedded Systems. Authors: W. Jiang (George Mason University).
10:30 - 11:00	Coffee Break				
10:10 - 12:30	Tutorial 1. Disruptive Memory Technologies: A Tutorial and Unified Simulation Framework. Authors: J.-J. Chen (TU Dortmund), J. Henkel (KIT), L. Siddhu (KIT).	Tutorial 2. Low Code, High Performance Embedded AI with MATLAB & Arm IP Explorer. Authors: B. Zhuang (MathWorks), A. Rajhans (MathWorks), E. Sondhi (Arm).	Tutorial 3. AMD's Ryzen AI Neural Processing Unit Hands-on Tutorial. Author: A. Schmidt (AMD).	Tutorial 4. Privacy Preserving Primitive for Health Data. Authors: F. Regazzoni (University of Amsterdam), P. Palmieri (University College Cork), A.P. Fournaris (ISI).	Tutorial 5. ARES: AI for Science on Resource-Constrained Embedded Systems. Authors: W. Jiang (George Mason University).
12:30 - 13:30	Lunch Break				

13:30 - 15:00	Tutorial 6. Large-Scale Spiking Neuromorphic Architectural Exploration using SANA-FE. Authors: J. Boyle, A. Gerstlauer (University of Texas at Austin).	Tutorial 7. Deploying Acoustic-Based Predictive AI for Machine Health using Model-Based Design Tools. Authors: B. Zhuang (MathWorks), A. Rajhans (MathWorks), T. Zhu (MathWorks).	Tutorial 8. Understand Your FPGA Designs Better: From Rapid Simulation to On-board Profiling. Authors: C. Hao (Georgia Institute of Technology), R. Sarkar (Georgia Institute of Technology), J. Kim (Georgia Institute of Technology).	Tutorial 9. Generative AI for Next-generation EDA Tool-flows. Authors: R. Karri (NYU), J.V. Rajendran (UT Austin), S. Garg (NYU).	Tutorial 10. Efficient Large Language Model Tuning on the Edge. Authors: Y. Chen (Duke University), T. Chen (University of Texas at Austin), J. Sun (Duke University).
15:00 - 15:30	Coffee Break				
15:30 - 17:00	Tutorial 6. Large-Scale Spiking Neuromorphic Architectural Exploration using SANA-FE. Authors: J. Boyle, A. Gerstlauer (University of Texas at Austin).	Tutorial 7. Deploying Acoustic-Based Predictive AI for Machine Health using Model-Based Design Tools. Authors: B. Zhuang (MathWorks), A. Rajhans (MathWorks), T. Zhu (MathWorks).	Tutorial 8. Understand Your FPGA Designs Better: From Rapid Simulation to On-board Profiling. Authors: C. Hao (Georgia Institute of Technology), R. Sarkar (Georgia Institute of Technology), J. Kim (Georgia Institute of Technology).	Tutorial 9. Generative AI for Next-generation EDA Tool-flows. Authors: R. Karri (NYU), J.V. Rajendran (UT Austin), S. Garg (NYU).	Tutorial 10. Efficient Large Language Model Tuning on the Edge. Authors: Y. Chen (Duke University), T. Chen (University of Texas at Austin), J. Sun (Duke University).
18:00 - 19:30	Reception				
Monday, September 30					
Oak Forest A+B					
08:30 - 09:00	Opening session				
09:00 - 10:00	KEYNOTE 1: Making tools to support the development of safety-critical embedded software Speaker: Jean-Louis Colaço (ANSYS) – Session chair: Alain Girault				
10:00 - 10:30	Coffee Break				
	Oak Forest B	Hannover I	Oak Forest A	Hannover II	Hannover III
10:30 - 12:00	CASES 1: Edge AI *	CODES+ISSS 1: Non-Volatile Memory and Storage * Session Chairs: Sudeep Pasricha	EMSOFT 1: Machine Learning under Resource Constraints Session Chair: Jian-Jia Chen	Special Session 1: Security-by-Design: Leveraging Security in Design of Hardware and Software for Embedded Hardware Systems Organizers: S.M. Pudukotai Dinakarao	

10:30 - 10:50	NDPGNN: A Near-data Processing Architecture for GNN Training and Inference Acceleration. * Best paper candidate. Authors: H. Wang, S. Zhang, X. Fan, Z. Yang, M. Zhang.	Reliable, Versatile, and Efficient Data Matching in SSD's NAND Flash Memory Chip for Data Indexing Acceleration. * Best paper candidate. Authors: Y. Chen, Y. Chang, T.-W. Kuo.	MII: A Multifaceted Framework for Intermittence-aware Inference and Scheduling. Authors: Z. Zhang, C. Liu, H. Kim.	Towards a Robust Metrology for Heterogeneous System-on-Chip Security. Author: G.P. Venkataramani.	
10:50 - 11:10	EASTER: Learning to Split Transformers at the Edge Robustly. Authors: X. Guo, Q. Jiang, Y. Shen, A. Pimentel, T. Stefanov.	AttentionRC: A Novel Approach to Improve Locality Sensitive Hashing Attention on Dual-addressing Memory. Authors: C.-L. Chu, Y.-C. Chen, W. Cheng, I.-C. Lin, Y.-H. Chang.	Batch-MOT: Batch-Enabled Real-Time Scheduling for Multi-Object Tracking Tasks. Authors: D. Kang, S. Lee, C. Hong, J. Lee, H. Baek.	Secure Embedded Systems' Design by Leveraging Hardware-Software Limitation and Interactions. Author: S.M. Pudukotai Dinakarrao.	
11:10 - 11:30	Deploy: Enabling Energy-Efficient Deployment of Small Language Models On Heterogeneous Microcontrollers. Authors: M. Scherer, L. Macan, V. Jung, P. Wiese, A. Burrello, F. Conti, L. Benini.	FIRM-tree: a Multidimensional Index Structure for Reprogrammable Flash Memory. Authors: S.-T. Wu, P.-J. Chen, P.-C. Huang, W.-K. Shih, Y.-H. Chang.	Arch2End: Two-stage Unified System-level Modeling for Heterogeneous Intelligent Devices. Authors: W. Liu, Z. Zhu, B. Li, Y. Xiong, Z. Lian, J. Geng, X. Zhou.	Snowflake IoT: Ultra-Low-Cost Diversity Defenses. Author: T. Austin.	
11:30 - 11:50	Efficient Batched Inference in Conditional Neural Networks. Authors: S. Selvam, A. Nagarajan, A. Raghunathan.	Near-Free Lifetime Extension for 3D NAND Flash via Opportunistic Self-Healing. Authors: T. Ren, Q. Li, Y. Lv, M. Ye, N. Guan, C. J. Xue.	CaBaFL: Asynchronous Federated Learning via Hierarchical Cache and Feature Balance. Authors: Z. Xia, M. Hu, D. Yan, X. Xie, T. Li, A. Li, J. Zhou, M. Chen.	Securing Large Monolithic Systems: Challenges and Opportunities. Author: A. Venkat.	
11:50 - 11:55	LB: Reducing ADC Front-end Costs During Training of On-sensor Printed Multilayer Perceptrons. Authors: F. Afentaki, P. Duarte, G. Zervakis, M. Tahoori.	Hardware and Software Co-design for Optimized Decoding Schemes and Application Mapping in NVM Compute-in-Memory Architectures.	LB: ML-based Fast and Precise Embedded Rack Detection Software for Docking and Transport of Autonomous Mobile Robots using 2D LiDAR. Authors: S. Hong, D. Park.		

11:55 - 12:00	LB: Energy-efficient Personalized Federated Continual Learning on Edge. Authors: Z. Yang, H. Wang, Q. Sun.	Authors: S.M. Siddaramu, A. Nezhadi, M. Mayahinia, S. Ghasemi, M. Tahoori.			
12:00 - 12:30	Poster Session				
12:30 - 13:30	Lunch Break				
	Oak Forest B	Hannover I (80)	Oak Forest A	Hannover II	Hannover III
13:30 - 15:00	CASES 2: AI Accelerators *	CODES+ISSS 2: Hardware-Software Co-Design * Session Chairs: Aman Arora and Rajesh Kedia	EMSOFT 2: Robot Operating Systems and Automotive Networks * Session Chair: Sanjoy Baruah	Special Session 2: Emerging Architecture Design, Control, and Security Challenges in Software Defined Vehicles (SDVs) Organizers: S. Pasricha and A.K. Singh	NSF Panel
13:30 - 13:50	A Dataflow-aware Network-on-Interposer for CNN Inferencing in the Presence of Defective Chiplets. * Best paper candidate. Authors: H. Sharma, U. Ogras, A. Kalyanaraman, P. Pande.	ROI-HIT: Region of Interest-driven High-dimensional Microarchitecture Design Space Exploration. * Best paper candidate. Authors: X. Zhao, T. Gao, A. Zhao, Z. Bi, C. Yan, F. Yang, S. G. Wang, D. Zhou, X. Zeng.	Dynamic Priority Scheduling of Multi-Threaded ROS 2 Executor with Shared Resources. Authors: A. Al Arafat, K. Wilson, K. Yang, Z. Guo.	Emerging In-Vehicle Architectures in the Age of SDV. Author: K. Shazzad.	
13:50 - 14:10	ARTEMIS: A Mixed Analog-Stochastic In-DRAM Accelerator for Transformer Neural Networks. Authors: S. Affi, I. Thakkar, S. Pasricha.	Bank on Compute-near-Memory: Design Space Exploration of Processing-near-Bank Architectures Authors: R.M. Morillas, G. Ansaloni, M. Zapater, A. Levisse, S.A. Chamazcoti, T. Evenblij, D. Biswas, F. Catthoor, D. Atienza.	Modelling and Analysis of the LatestTime Message Synchronization Policy in ROS. Authors: C. Wu, R. Li, N. Zhan, N. Guan.	New Paradigms for Automotive Control in the Era of SDV. Author: S. Chakraborty.	

14:10 - 14:30	AxOSpike: Spiking Neural Networks-driven Approximate Operator Design. Authors: S. Ullah, S. Sahoo, A. Kumar.	EQ-ViT: Algorithm-Hardware Co-Design for End-to-End Acceleration of Real-Time Vision Transformer Inference on Versal ACAP Architecture Authors: P. Dong, J. Zhuang, Z. Yang, S. Ji, Y. Li, D. Xu, H. Huang, J. Hu, A.K. Jones, Y. Shi, Y. Wang, P. Zhou.	Thread Carefully: Preventing Starvation in the ROS 2 Multithreaded Executor. * Best paper candidate. Authors: H. Teper, D. Kuhse, M. Guenzel, G. von der Brüggen, F. Howar, J. Chen.	Emerging Robustness: Robust Perception with Embedded Systems in SDVs. Author: S. Pasricha.	
14:30 - 14:50	Efficient Image Processing via Memristive-based Approximate In-Memory Computing. Authors: F. Seiler, N. TaheriNejad.	NeRF-PIM: PIM Hardware-Software Co-design of Neural Rendering Networks Authors: J. Heo, S. Yoo.	Large Data Transfer Optimization for Improved Robustness in Real-Time V2X-Communication. Authors: A. Bendrick, N. Sperling, R. Ernst.	Emerging Security: Covert Channel and In-vehicle Network Spoofing Attacks on Embedded Systems in SDVs. Author: A.K. Singh.	
14:50 - 14:55	LB: ViTSen: Bridging Vision Transformers and Edge Computing with Advanced In/Near-Sensor Processing. Authors: S. Tabrizchi, B. Reidy, D. Najafi, S. Angizi, R. Zand, A. Roohi.	LB: Co-designing Perception-based Autonomous Systems on CPU-GPU platforms Authors: S. Singh, A. R. Molla, A. Mondal, S. Dey.	WiP: Development of Margin-shared System-level Logical Execution Time Simulator to Support Scheduling Design of Automotive ECUs. Authors: M. Mizoguchi, Y. Kato, K. Yoshimura, T. Nokaido, Y. Ikeda, H. Sakamoto.		
14:55 - 15:00	LB: HDVQ-VAE: Binary Codebook for Hyperdimensional Latent Representations. Authors: A. Bryant, S. Aygun.	LB: FDPFS: Leveraging File System Abstraction for FDP SSD Data Placement Authors: P.-X. Chen, D. Seo, N. Dutt.	WiP: Real-Time Vehicular Traffic-Based Crowd Density Estimation for Reducing Epidemiological Risks. Authors: S. Alhazmi, S. Lowy, A. Cheng.		
15:00 - 15:30	Poster Session & Coffee Break				
15:30 - 17:00	CASES 3: Security meets Embedded Systems *	CODES+ISSS 3: Security and Reliability * Session Chairs: Andreas Gerstlauer and Fareena Saqib	EMSOFT 3: Cyber-Physical Systems * Session Chair: Pierluigi Nuzzo	Special Session 3: Design for Environmental Sustainability in Computing Organizers: J. Hu and P. Zhou	PhD forum and Recruitment event

15:30 - 15:50	<p>MaskedHLS: Domain-Specific High-Level Synthesis of Masked Cryptographic Designs. *</p> <p>Best paper candidate. Authors: N. Sarma, A. Thakur, C. Karfa.</p>	<p>Flexible Generation of Fast and Accurate Software Performance Simulators from Compact Processor Descriptions. *</p> <p>Best paper candidate. Authors: C. Foik, R. Kunzelmann, D. Mueller-Gritschneider, U. Schlichtmann.</p>	<p>Statistical Reachability Analysis of Stochastic Cyber-Physical Systems under Distribution Shift.</p> <p>Authors: N. Hashemi, L. Lindemann, J. Deshmukh.</p>	<p>Modeling and Optimizing the Carbon Objective for Sustainable Architectures and Systems.</p> <p>Author: A.K. Jones.</p>	
15:50 - 16:10	<p>Balancing Security and Efficiency: System-Informed Mitigation of Power-Based Covert Channels.</p> <p>Authors: J. Gonzalez-Gomez, M. Sikal, L. Bauer, H. Khdr, J. Henkel.</p>	<p>HMC-FHE: A Heterogeneous Near Data Processing Framework for Homomorphic Encryption.</p> <p>Authors: Z. Chen, Z. Cao, Z. Shen, L. Ju.</p>	<p>Analysis and Prevention of MCAS-Induced Crashes. *</p> <p>Best paper candidate. Authors: N. Curran, T. Kennings, K. Shin.</p>		
16:10 - 16:30	<p>TPE-Det: A Tamper-Proof External Detector via Hardware Traces Analysis against IoT Malware.</p> <p>Authors: N. Yamin, G. Bhat.</p>	<p>Meta-Scanner: Detecting Fault Attacks via Scanning FPGA Designs Metadata.</p> <p>Authors: H. Nassar, J. Krautter, L. Bauer, D.R.E. Gnad, M. Tahoori, J. Henkel.</p>	<p>Revisiting Dynamic Scheduling of Control Tasks: A Performance-aware Fine-grained Approach.</p> <p>Authors: S. Adhikary, I. Koley, S. Ghosh, S. Ghosh, S. Dey.</p>	<p>Sustainable Deployment of Deep Neural Networks on Non-Volatile Compute-in-Memory Accelerators.</p> <p>Author: Y. Shi.</p>	
16:30 - 16:50	<p>Formal Verification of Virtualization-based Trusted Execution Environments.</p> <p>Authors: H. Witharana, H. Weerasena, P. Mishra.</p>	<p>Latent RAGE: Randomness Assessment using Generative Entropy Models.</p> <p>Authors: K. Pratihar, R.S. Chakraborty, D. Mukhopadhyay.</p>	<p>Backdoor Attacks on Safe Reinforcement Learning-Enabled Cyber-Physical Systems.</p> <p>Authors: S. Jiang, M. Liu, F. Kong.</p>		
16:50 - 16:55	<p>LB: A Novel Insight into the Vulnerability of DDR4 DRAM Cells Across Multiple Hammering Settings.</p> <p>Authors: R. Zhou, J. Liu, N. Kochar, S. Ahmed, A. Rakin, S. Angizi.</p>	<p>Enhancing SRAM-Based PUF Reliability Through Machine Learning-Aided Calibration Techniques.</p>	<p>LB: Towards Precision-Aware Safe Neural-Controlled Cyber-Physical Systems.</p> <p>Authors: H. Thevendhriya, S. Ghosh, D. Lohar.</p>	<p>End-To-End Carbon Footprint Assessment and Modeling of Deep Learning</p>	

16:55 - 17:00	WiP: ACPO: An AI-Enabled Compiler Framework. Authors: A. Ashouri, M. Manzoor, D. Vu, R. Zhang, Z. Wang, A. Zhang, B. Chan, T. Czajkowski, Y. Gao.	Authors: K. Pratihari, S. Chatterjee, R.S. Chakraborty, D. Mukhopadhyay.		Deep Learning. Author: F. Chen.	
17:00 - 17:30	Poster Session				
	Tuesday, October 1				
	Oak Forest A+B				
08:30 - 09:00	Test of Time Award Ceremony				
09:00 - 10:00	KEYNOTE 2: How Computational Infrastructure is Changing the Planet (for Better and for Worse). And How Planetary Thinking Might Shift How We Do Computational Infrastructure. Speaker: Prof. Steven J. Jackson (Cornell) – Session chair: Sharon Hu				
10:00 -10:30	Coffee Break				
	Oak Forest B	Hannover I	Oak Forest A	Hannover II	
10:30 - 12:00	CASES 4: Memory and Storage Systems	CODES+ISSS 4: Acceleration of Neural Networks Session Chairs: Soonhoi Ha and Jason Xue	EMSOFT 4: Verification and Scheduling for Learning-Enabled Systems * Session Chair: Borzoo Bonakdarpour	Embedded Systems Software Competition (ESSC) Organizers: Bires Kumar Joardar and Ganapati Bhat	
10:30 - 10:50	LightFS: A lightweight host-CSD coordinated file system optimizing for heavy small file accesses. Authors: J. Li, Z. Shen, D. Liu, X. Chen, K. Zhong, Z. Zeng, Y. Tan.	FlexBCM: Hybrid Block-Circulant Neural Network and Accelerator Co-Search on FPGAs Authors: W. Lou, Y. Qin, X. Wang, L. Gong, C. Wang, X. Zhou.	Interval Image Abstraction for Verification of Camera-Based Autonomous Systems. Authors: Habeeb P, D. D'Souza, K. Lodaya, P. Prabhakar.		
10:50 - 11:10	NICE: A Non-intrusive In-Storage-Computing Framework for Embedded Applications. Authors: T. Wang, Y. Zhu, S. Li, J. Xue, C. Ma, Y. Wang, Z. Shen, Z. Shao.	OPIMA: Optical Processing-In-Memory for Convolutional Neural Network Acceleration Authors: F. Sunny, A. Shafiee, A. Balasubramaniam, M. Nikdast, S. Pasricha.	Polynomial Neural Barrier Certificate Synthesis of Hybrid Systems via Counterexample Guidance. * Best paper candidate. Authors: H. Zhao, B. Liu, L. Dehbi, H. Xie, Z. Yang, H. Qian.		

11:10 - 11:30	NOVELLA: Non-Volatile Last-Level Cache Bypass for Optimizing Off-chip Memory Energy. Authors: A. Bagchi, O. Rishabh, P. Panda.	Training on the Fly: On-device Self-supervised Learning aboard Nano-drones within 20mW. Authors: E. Cereda, A. Giusti, D. Palossi.	BERN-NN-IBF: Enhancing Neural Network Bound Propagation Through Implicit Bernstein Form and Optimized Tensor Operations. Authors: W. Fatnassi, A. Feeney, V. Yamamoto, A. Chandramowliswaran, Y. Shoukry.		
11:30 - 11:50	NOBtree: A NUMA-Optimized Tree Index for Non-Volatile Memory. Authors: Z. Chu, P. Jin, Y. Luo, X. Wang, S. Wan.	FlexFL: Heterogeneous Federated Learning via APoZ-Guided Flexible Pruning in Uncertain Scenarios. Authors: Z. Chen, C. Jia, M. Hu, X. Xie, A. Li, M. Chen.	VALO: A Versatile Anytime Framework For LiDAR based Object Detection Deep Neural Networks. Authors: A. Soyyigit, S. Yao, H. Yun.		
11:50 - 11:55	LB: MUSIC-lite: Efficient MUSIC using Approximate Computing: An OFDM Radar Case Study. Authors: R. Bhattacharjya, A. Sarkar, B. Maity, N. Dutt.	LB: Heterogeneous Accelerator Design for Multi-DNN Workloads via Heuristic Optimization. Authors: K. Balaskas, H. Khdr, M. B. Sikal, F. Kreß, K. Siozios, J. Becker, J. Henkel.	LB: An Explainable and Formal Framework for Hypertension Monitoring using ECG and PPG. Authors: A. Panda, A. Anand, S. Pinisetty, P. Roop.		
11:55 - 12:00	LB: Novel Toolset for Efficient Hardwired Micro-Op Translation in Embedded Microarchitectures. Authors: K. Phillipson, M. Rywalt, B. Chatterjee, E. Schwartz, G. Stitt.	LB: Characterizing CNN Throughput and Energy Under Multi-threaded and Multi-accelerator Execution. Authors: M.A. Muneeb, R. Kedia.	WiP: On-device Retrieval Augmented Generation with Knowledge Graphs for Personalized Large Language Models. Authors: C. Lee, D. Prahlad, D. Kim, H. Kim.		
12:00 - 12:30	Poster Session				
12:30 - 13:30	Lunch Break				
	Oak Forest B	Hannover I	Oak Forest A	Hannover II	
13:30 - 15:00	CASES 5: Hardware and Software Co-Design	CODES+ISSS 5: Domain-Specific Optimizations Session Chairs: Preeti Ranjan Panda and Aviral Shrivastava	EMSOFT 5: Cyber-Security Session Chair: Alessandro Biondi	ACM Students Research Competition (SRC) Organizer: Wanli Chang	

13:30 - 13:50	Indoor-Outdoor Energy Management for Wearable IoT Devices with Conformal Prediction and Rollout. Authors: N. Yamin, G. Bhat.	SCIMITAR: Stochastic Computing In-Memory In-situ Tracking ARchitecture for Event-Based Cameras. Authors: W. Romaszkan, J. Yang, A. Graening, V.K. Jacob, J. Sen, S. Pamarti, P. Gupta.	ECG: Augmenting Embedded Operating System Fuzzing via LLM-based Corpus Generation. Authors: Q. Zhang, Y. Shen, J. Liu, Y. Xu, H. Shi, W. Chang, Y. Jiang.		
13:50 - 14:10	FreePrune: An Automatic Pruning Framework Across Various Granularities Based on Training-free Evaluation. Authors: M. Tang, N. Liu, T. Yang, H. Fang, Q. Lin, Y. Tan, X. Chen, D. Liu, K. Zhong, A. Ren.	Implementing Oversized Neural Network on Nonvolatile FPGAs. Authors: H. Zhang, J. Zuo, H. Zheng, S. Liu, M. Luo, M. Zhao.	Caphammer: Exploiting Capacitor Vulnerability of Energy Harvesting Systems. Authors: J. Choi, J. Choi, H. Joe, C. Jung.		
14:10 - 14:30	NebulaFL: Self-Organizing Efficient Multi-Layer Federated Learning Framework with Adaptive Load Tuning in Heterogeneous Edge Systems. Authors: Z. Lian, J. Cao, Q. Cao, Z. Zhu, W. Liu, X. Zhou.	Detecting Spoofed Noisy Speeches via Activation-Based Residual Blocks for Embedded Systems. Authors: J. Zhan, S. Peng, W. Jiang, X. Wang, J. Liu.	Untrusted Code Compartmentalization for Bare Metal Embedded Devices. Authors: L. Tyler, I. Nunes.		
14:30 - 14:50	Domain-Adaptive Online Active Learning for Real-Time Intelligent Video Analytics on Edge Devices. Authors: M. Boldo, M. De Marchi, E. Martini, S. Aldegheri, N. Bombieri.	EMI: Energy Management meets Imputation in Wearable IoT Devices. Authors: D. Hussein, N. Yamin, G. Bhat.	Parallel Fuzzing of IoT Messaging Protocols through Collaborative Packet Generation. Authors: Z. Luo, J. Yu, Q. Du, Y. Zhao, F. Wu, H. Shi, W. Chang, Y. Jiang.		
14:50 - 14:55	LB: FPonAP: Implementation of Floating Point Operations on Associative Processors. Authors: W. Amer, M. Rakka, F. Kurdahi.	LB: Dynamic Segmented Bus for Energy-efficient Last-level Cache in Advanced Interconnect-dominant Nodes. Authors: M. Mayahinia, T. Marinelli, Z. Pei, H.-H. Liu, C. Pan, Z. Tokei, F. Catthoor, M. Tahoori.	LB: Run-Time ROP Attack Detection on Embedded Devices Using Side Channel Power Analysis. Authors: J. Xu, D. Abraham, I. Harris.		

14:55 - 15:00	WiP: Temporal RegionDrop -- Frame Difference Sparsity for Efficient Video Inference. Authors: Y. Sada, S. Shibata, Y. Kobayashi, T. Takenaka.	LB: MetaTinyML: End-to-End Metareasoning Framework for TinyML Platforms. Authors: M. Navardi, E. Humes, T. Mohsenin.			
15:00 - 15:30	Poster Session & Coffee Break				
	Oak Forest A+B				
15:30 - 17:00	Panel 1: The embedded systems and the environmental crisis				
17:00 - 18:00	Competition Demo Session				
19:30 - 23:00	Social Event				
	Wednesday, October 2				
	Oak Forest A+B				
08:30 - 09:00	Best Paper Award Ceremony				
09:00 - 10:00	KEYNOTE 3: Embedded Exponentials: Milestones, Momentum, and the Frontier Speaker: Prof. Tulika Mitra (NUS) -- Session chair: Tei-Wei Kuo				
10:00 - 10:30	Coffee Break				
	Oak Forest B	Hannover I	Oak Forest A	Hannover II	
10:30 - 12:00	CASES 6: Security meets Embedded Systems	CODES+ISSS 6: Performance and Reliability Session Chairs: Andy Pimentel	EMSOFT 6: Systems Session Chair: Cong Liu	Special Session 4: Estimation and Optimization of DNNs for Embedded Platforms Organizers: A. Jantsch, S. Han, L. Meng, and O. Bringmann	
10:30 - 10:50	FDPUF: Frequency-Domain PUF for Robust Authentication of Edge Devices. Authors: S. Paul, A. Dasgupta, S. Bhunia.	CHEF: A Framework for Deploying Heterogeneous Models on Clusters with Heterogeneous FPGAs. Authors: Y. Tang, Y. Song, N. Elango, S.R. Priya, A.K. Jones, J. Xiong, P. Zhou, J. Hu.	KPAC: Efficient Emulation of the ARM Pointer Authentication Instructions. Authors: I. Ostapyshyn, G. Serra, T. Thomas, D. Lohmann.	Visual Language Models for Edge AI 2.0. Author: S. Han.	

10:50 - 11:10	SENTINEL: Securing Indoor Localization against Adversarial Attacks with Capsule Neural Networks. Authors: D. Gufran, P. Anandathirtha, S. Pasricha.	High-Performance Remote Data Persisting for Key-Value Stores via Persistent Memory Region. Authors: Y. Luo, P. Jin, X. Wang, Z. Chu, K. Guo, J. Guo, P. Xu, F. Liu.	iFKVS: Lightweight Key-Value Store for Flash-Based Intermittently-Computing Devices. Authors: Y. Chen, T. Liao, L. Chang.	DNN Model Optimization and Implementation for Embedded Systems. Author: L. Meng.	
11:10 - 11:30	Multi-Mode Security-Aware Real-Time Scheduling on Multiprocessors. Authors: J. Ren, C. Liu, C. Lin, W. Jiang, P. Wang, X. Qi, S. Li, S. Li.	PARS: A Pattern-Aware Spatial Data Prefetcher Supporting Multiple Region Sizes. Authors: Y. Lin, W. Lin, J. Xu, Y. Chen, Z. Jin, J. Qin, J. He, S. Cai, Y. Zhang, Z. Wang, W. Chen.	D-Linker: Debloating Shared Libraries by Relinking From Object Files. Authors: J. He, P. Hou, J. Yu, J. Qi, Y. Sun, L. Li, R. Zhao, Y. Wu.	Latency estimation. Author: A. Jantsch.	
11:30 - 11:50	Learning Memory Contention Timing Models With Automated Platform Profiling. Authors: A. Stevanato, M. Zini, A. Biondi, A. Biasci, B. Morelli.	GEAR: Graph-Evolving Aware Data ArrangeR to Enhance the Performance of Traversing Evolving Graphs on SCM. Authors: W.-Y. Wang, C.-F. Wu, Y.-C. Chen, T.-W. Kuo, Y.-H Chang.	Ghostbuster: A Software Approach for Reducing Ghosting Effect on Electrophoretic Displays. Authors: T. Hu, M. Cui, M. Lyu, T. Yang, Y. Zhou, Q. Deng, C. Xue, N. Guan.	Multi-level Performance Estimation of Multi-instance AI Compute Platforms. Author: O. Bringmann.	
11:50 - 11:55	LB: SPELL: An End-to-End Tool Flow for LLM-Guided Secure SoC Design for Embedded Systems. Authors: S. Paria, A. Dasgupta, S. Bhunia.	LB: Enhancing HLS Performance Prediction on FPGAs through Multi-Modal Representation Learning. Authors: L. Shang, T. Wang, L. Gong, C. Wang, X. Zhou.	WIP: ESops - An Agile Pipeline for Next-Generation Embedded Systems Development. Authors: M. Al Maruf, A. Azim.		
11:55 - 12:00	LB: Hiding in Plain Sight: Reframing Hardware Trojan Benchmarking as a Hide&Seek Modification. Authors: A. Sarihi, A. Patooghy, P. Jamieson, A. Badawy.	LB: MONO: Enhancing Bit-Flip Resilience with Bit Homogeneity for Neural Networks. Authors: M. Eslami, Y. Liu, S. Ullah, M.E.S. Nasab, R. Hosseini, S.A. Mirsalari, A. Kumar.			
12:00 - 12:30	Poster Session				
12:30 - 13:30	Lunch Break				
	Oak Forest B	Hannover I	Oak Forest A	Hannover II	

13:30 - 15:00	CASES 7: Architectures and Embedded Systems	COSES+ISSS 7: It's All about Time Session Chairs: Amit Kumar Singh and Soumyajit Dey	EMSOFT 7: Formal Methods and Verification Session Chair: Timothy Bourke	Special Session 5: Neuro-Symbolic Architecture Meets Large Language Models: A Memory-Centric Perspective Organizers: M. Ibrahim, Z. Wan, C.-K. Liu, A. Raychowdhury	
13:30 - 13:50	Page Type-aware Full-sequence Program Scheduling via Reinforcement Learning in High Density SSDs. Authors: J. Li, Z. Cai, B. Gerofi, Y. Ishikawa, J. Liao.	ML-Based Thermal and Cache Contention Alleviation on Clustered Manycores with 3D HBM. Authors: M.B. Sikal, H. Khdr, L. Siddhu, J. Henkel.	Hyper parametric timed CTL. Authors: M. Waga, É. André.	Biologically Inspired Computing Architectures and Circuits for Embodied Intelligence. Author: A. Raychowdhury.	
13:50 - 14:10	DREAMx: A Data-driven Error Estimation Methodology for Adders Composed of Cascaded Approximate Units. Authors: M. Hanif, A. Arous, M. Shafique.	HuNT: Exploiting Heterogeneous PIM Devices to Design a 3D Manycore Architecture for DNN Training. Authors: C. Ogbogu, G. Narang, B.K. Joardar, J.R. Doppa, K. Chakrabarty, P.P. Pande.	Contract-Based Hierarchical Modeling and Traceability of Heterogeneous Requirements. Authors: N. Naik, A. Pinto, P. Nuzzo.	Efficient LLMs: Innovations in Quantization, Memory, and Attention. Author: P. Panda.	
14:10 - 14:30	GOURD: Tensorizing Streaming Applications to Generate Multi-instance Compute Platforms. Authors: P. Schmid, P. Bernardo, C. Gerum, O. Bringmann.	Time-Triggered Scheduling for Non-Preemptive Real-Time DAG Tasks Using 1-Opt Local Search. Authors: S. Wang, D. Li, S. Huang, X. Deng, A.H. Sifat, J.-B. Huang, C. Jung, R.K. Williams, H. Zeng.	Efficient Discovery of Actual Causality using Abstraction-Refinement. Authors: A. Rafieioskouei, B. Bonakdarpour.	Energy-Efficient Computational Memories as Heterogenous CMOS+X Platforms for Neuro-Symbolic and Transformer Architectures. Author: H. Li.	
14:30 - 14:50	GPU Performance Optimization via Inter-group Cache Cooperation. Authors: G. Wang, Y. Du, W. Huang.	Runtime Monitoring of ML-based Scheduling Algorithms toward Robust Domain-Specific SoCs. Authors: A.A. Goksoy, A. Kanani, S. Chatterjee, U.Y. Ogras.	Approximate Conformance Checking for Closed-Loop Systems with Neural Network Controllers. Authors: Habeeb P, L. Gupta, P. Prabhakar.	Von Neumann-like Architecture for Computing with High-Dimensional Vectors Motivated by Neuroscience and Psychology. Author: P. Kanerva.	

14:50 - 14:55	HLS-based Approach for Embedded Real-Time Ray-Tracing in Wireless Communications. Authors: J. An, S. Saidi.	WiP: Worst-Case Execution-Time Measurement Techniques for Nonlinear Model Predictive Controllers. Authors: R. Krishnamurthy, G.A. Perez, J. Denil, W. Goossens.	LB: Methodology for formal verification of hardware safety strategies using SMT. Authors: A. Faure-Gignoux, K. Delmas, A. Gauffriau, C. Pagetti.	The Application of Spiking Neural Networks (SNNs) in Large Language Models and Their Implementation with Compute-in-Memory (CIM). Author: Y. Chen.	
14:55 - 15:00		WiP: Context and Noise Aware Resilience for Autonomous Driving Applications. Authors: H. Alikhani, A. Kanduri, P. Liljeberg, A.M. Rahmani, N. Dutt.			
15:00 - 15:30	Poster Session & Coffee Break				
	Oak Forest A+B				
15:30 - 17:00	Panel 2: Celebrating 20 years of ESWeek				
17:00 - 17:30	Closing session				
	Thursday, October 3				
	Hannover I	Hannover II	Hannover III	Capital	
08:30 - 09:00	Welcome speech Srinivas Pinisetty				
09:00 - 09:30	MEMOCODE Keynote 1 Towards a Design Flow for Verified AI-Based Autonomy Speaker: S.A. Seshia (UC Berkeley).		RSP 1: Crypto Session Chair: Tobias Strauch. Decoding Attack Behaviors by Analyzing Patterns in Instruction-Based Attacks using gem5 Authors: M. Awais, M. Mushtag, L. Naviner, F. Bruguier, J. H. Yahya, P. Benoit.	MSC Keynote Desktop Swap on Mobile Device: Is it a Good Idea? Speaker: L.-P. Chang (National Yang Ming Chiao Tung University).	
09:30 - 10:00			Temporal Staging for Correct-by-Construction Cryptographic Hardware Authors: Y. Forman, W. Harrison.		
10:00 - 10:30	Coffee Break				

10:30 - 12:30	MEMOCODE 1: Formal Verification and Monitoring *	TCRS 1: Coordinating Time-Sensitive Dynamic Systems	RSP 2: Hardware Session Chair: K. Kent	MSC 1: Design and Optimization for Memory and Storage Systems	
10:30 - 11:00	Fast Robust Monitoring for Signal Temporal Logic with Value Freezing Operators (STL*). * Best paper candidate Authors: B. Ghorbel, V. Prabhu.	Layered Scheduling: Toward Better Real-Time Lingua Franca. Authors: F. Paladino, E. Jellum, E. Soyer, E.A. Lee.	Invited Talk: Circuit Partitioning with Reinforcement Learning and Edge-Based Initialization. Authors: K.C. Cheng, U. F. Siddigi, G. Grewal, S.M. Areibi.	(10:30-11:10) Read Retry Mechanism for 3D NAND Flash Memory: Observations, Analyses, and Solutions. Author: J.-W. Hsieh.	
11:00 - 11:30	Modelling and proving pipeline monotonicity in Coq. * Best paper candidate Authors: A. Gruin, A. Bonenfant, T. Carle, C. Rochange.	Toward Dynamism in Distributed Lingua Franca Programs. Authors: C. Jerad, E.A. Lee.	Advancing Formal Verification: Fine-Tuning LLMs for Translating Natural Language Requirements to CTL Specifications. Authors: R. Zrelli, H. A. Misson, M. Ben Attia, F. Gohring de Magalhaes, A. Shabah, G. Nicolescu.	(11:10-11:50) When Memory-Storage Systems Go Unconventional: Some Techniques and Thoughts. Author: P.-C. Huang.	
11:30 - 12:00	Perception-based Runtime Monitoring and Verification for Human-Robot Construction Systems. * Best paper candidate Authors: A. Pramanik, S. W. Choi, Y. Li, L. Nguyen, K. Kim, D.H. Tran.	Navigating Time and Energy Trade-offs in Reactive Heterogeneous Systems. Authors: S. Lin, T. Tanneberger, J. Bi, G. Feng, R. Xu, J. Robledo, R. Khasanov, J. Castrillon.	Transaction Level Hierarchy Guided and Functional Coverage Driven Deductive Formal Verification. Authors: T. Strauch.	(11:50-12:30) Achieving High-Performance Out-of-Core Graph Processing with I/O Optimizations. Author: T.-Y. Yang.	
12:00 - 12:30	Safety and Progress Proofs of Reactive Autonomous Racing Algorithm. Authors: A. Karimi, M. Goyal, P. S. Duggirala.	Lustre, Fast First and Fresh. Authors: T. Bourke, M. Pouzet.	Cost-Effective Cyber-Physical System Prototype for Precision Agriculture with a Focus on Crop Growth. Authors: P. Kumar, H. Kim.		
12:30 - 13:30	Lunch Break				
13:30 - 15:00	MEMOCODE 2: Learning-based Systems			MSC 2: Pearls on Tool Chains of In-Memory Computing	

13:30 - 14:00	Model-free PAC Time-Optimal Control Synthesis with Reinforcement Learning. Authors: M. Liu, P. Lu, X. Chen, F. Kong, O. Sokolsky, I. Lee.	TCRS + RSP: Joint Keynote (Room: Hannover II) Certification of (hybrid) multi-core architectures Speaker: C. Pagetti (Onera)	Towards Energy-Efficient Memory-Centric Computer Architectures: A Design Tool Perspective. Author: Z. Zhu.	
14:00 - 14:30	Exploring Compositional Neural Networks for Real-Time Systems. Authors: S. Chatterjee, N. Allen, N. Patel, P. Roop.		In-Memory Computing Low Level Programming Model and Compiler Innovation. Author: H.-P. Charles.	
14:30 - 15:00	MaLT: Machine-Learning-Guided Test Case Design and Fault Localization of Complex Software Systems. Authors: Y. Ji, S. Mak, R. Lekivetz, J. Morgan.		In-Memory Computing Research and Development: Status and Perspectives. Author: W. Kang.	
15:00 - 15:30	Coffee Break			
15:30 - 17:00	MEMOCODE 3: Invited Session	TCRS 2: Timing Challenges in Cyber-Physical Systems	RSP 3: Synthesis Flow and Performance Evaluation Session Chair: F. Magalhaes	
15:30 - 16:00	Logical Synchrony + Functional Processes => Observable Determinacy. Authors: S. Prasad.	Software-Defined Watchdog Timers for Cyber-Physical Systems. Authors: B. Asch, E. Jellum, M. Lohstroh, E.A. Lee.	Non-interfering On-line and In-field SoC Testing. Authors: T. Strauch.	
16:00 - 16:30	Self-Powering Dataflow Networks – Concepts and Implementation. Authors: A. Karim, J. Falk, D. Schmidt, J. Teich.	Time-Sensitive Networking in Cyber-Physical Systems. Authors: H. Austad, G. Mathisen.	Page size exploration for RISC-V systems: the case for HPC. Authors: E.T. Ribeiro, C. Fuguet, C. Fabre, F. Pétrot.	
16:30 - 17:00	Neuro-symbolic Generative AI Assistant for System Design. Authors: S. Jha, S.K. Jha, and S. Velasquez.	GNN-MiCS: Graph Neural-Network-Based Bounding Time in Embedded Mixed-Criticality Systems. Authors: B. Ranjbar, P. Justen, A. Kumar.	Enhancing the VTR Flow: Integration of ABC9 via Yosys for Better Technology Mapping and Optimization. Authors: N. Jafarof, K. Kent.	

Friday, October 4					
	Hannover I	Hannover II	Hannover III		
09:00 - 10:00	MEMOCODE Keynote 2 From Neural Network Verification to Formal Verification for Neuro-Symbolic Artificial Intelligence (AI). Author: T.T. Johnson (Vanderbilt University).		Welcome Speech: X. Zheng, A.K. Mok, A. Khazraei, M. Pajic. TACPS Keynote Safety Verification via Deep Learning. Author: S. Baruah (Washington University in St. Louis).		
10:00 - 10:30	Coffee Break				
10:30 - 12:30	MEMOCODE 4: Hardware/CPS Verification	LLM-PIM 1 Chair: Z. Zhu	TACPS 1 Chair: R. Piskac		
10:30 - 11:00	Formal Fault Injection in Digital Blocks with Mined Assertions. Authors: D. Zuccala, P. Breuil, J. Daveau, P. Roche, K. Morin-Allory.	Keynote 1 Enhancing Resilience of In-Memory Computing to Device Variations. Speaker: S. Hu (Notre Dame).	Invited Talk 1 (10:30 - 11:15) How Safe Will I Be Given What I See? Visual Prediction of Calibrated Safety Chances with (Foundation) World Models. Author: I. Ruchkin.		
11:00 - 11:30	Higher-order Hardware: Implementation and Evaluation of The Cephalopode Graph Reduction Processor. Authors: J. Pope, C.H. Seger, H. Valter.		Invited Talk 2 (11:15 - 12:00) Behavioral Testing and Certification of Autonomous Vehicles. Author: P.S. Duggirala.		
11:30 - 12:00	Physics-Aware Mixed-Criticality Systems Design via End-to-End Verification of CPS. Authors: K. Wilson, A. Al Arafat, J. Baugh, R. Yu, Z. Guo.	Keynote 2 3D Integrated Computing-In-Memory Chips			

12:00 - 12:30	Configuring Safe Spiking Neural Controllers for Cyber-Physical Systems through Formal Verification. Authors: A. Gupta, S. Ghosh, A. Banerjee, S.K. Mohalik.	Memory Chips. Speaker: B. Gao (Tsinghua University).	Dagstuhl and Shonan seminar preparation and discussion. Moderator: X. Zheng.		
12:30 - 13:30	Lunch Break				
13:30 - 15:00	MEMOCODE 5: WiP - Distributed systems, Sensor fusion, Statecharts	LLM-PIM 2 Chair: Z. Zhu	TACPS 2 Chair: M. Pajic		
13:30 - 14:00	Safety Assurance for Autonomous Systems with Multiple Sensor Modalities. Authors: A. Balakrishnan, R. Bernard, S. Narayanan, V. Kudalkar, Y. Zhao, P. Nagaraja, G. Markov, C. Budnik, H. Degen, L. Lindemann, J.V. Deshmukh.	Invited Talk 1 (13:30 - 14:15) Energy Efficient 3D Heterogeneous Many-core Architecture for Transformer Acceleration. Author: P. Dhingra.	Invited Talk 3 (13:30 - 14:15) Formal Methods for Accountable Cyber-Physical Systems. Author: R. Piskac.		
14:00 - 14:30	Efficient Coordination for Distributed Discrete-Event Systems. Authors: B. Jun, E.A. Lee, M. Lohstroh, H. Kim.	Invited Talk 2 (14:15 - 15:00) SRAM based Computation in Memory Circuits Design for Edge CNNs and Transformers. Author: X. Si.	Invited Talk 4 (14:15 - 15:00) Engineering safe autonomous systems: achievements and challenges. Author: E. Troubitsyna.		
14:30 - 15:00	Pragmatic Action Charts. Author: S. Smyth.				
15:00 - 15:30	Coffee Break				
15:30 - 17:30		LLM-PIM 3 Chair: Z. Zhu	TACPS 3 Chair: X. Zheng.		
15:30 - 16:15		Invited Talk 3 Exploring Flex-Enabled Reconfigurable Processor-in-Memory Architectures for Data intensive Applications. Author: S. Bavikadi.	Invited Talk 5 Current Trends in Neuro-Symbolic Paradigm. Author: A. Solar-Lezama.		

16:15 - 17:00		Invited Talk 4 Drainage: A Multi-task Coroutine Management Mechanism for Computational Storage. Author: X. Chen.	Panel Discussion On the impact of foundation models and the neuro-symbolic paradigm on trusted autonomy. Panelists: I. Ruchkin, M. Pajic, A. Solar-Lezama.		
17:00 - 17:15		Closing Remarks			