## Brief Contents

**Welcome Message**  
Info-2  

**Committees**  
Info-4  

**Reviewers**  
Info-10  

### Keynote Talks

| Keynote I | Skin-Like Wireless Wearables-From Premature Babies in the NICU to Patients with COVID-19  
**John A. Rogers**  
Info-13 |
|---|---|
| Keynote II | Digital Twins: Challenges and Opportunities in Various Industries  
**Prith Banerjee**  
Info-14 |
| Panel | Post COVID-19 Cyber Security: The Challenges and Solutions  
**Sri Parameswaran**  
Info-16 |

### Tutorials

| Tutorial I | Creating Domain-Specific Modeling Languages: Hands-on  
**Juha-Pekka Tolvanen and Steven Kelly**  
Info-18 |
|---|---|
| Tutorial II | Software-Defined Hardware: Digital Design with Chisel  
**Martin Schoberl**  
Info-19 |
| Tutorial III | Out-of-Order Parallel Simulation of SystemC Models using the RISC Framework  
**Rainer Diemer**  
Info-20 |
| Tutorial IV | Tasking Framework: An open-source software development library for on-board software systems  
**Zain A. H. Hammadeh and Olaf Maibaum**  
Info-21 |

### Conferences Technical Programme

| Day 1 — Monday, 21 September 2020 | 1 |
| Day 2 — Tuesday, 22 September 2020 | 7 |
| Day 3 — Wednesday, 23 September 2020 | 14 |
| Day 3 — Wip Papers, September 2020 | 20 |
Welcome to the Virtual edition of ESWEEK 2020!

Due to the pandemic, this 16th edition of ESWEEK is a unique and non-traditional, but still very exciting and engaging event. ESWEEK 2020 is fully virtual this year. It consists of short live sessions every day that, together with a very low registration fee, provide an unprecedented opportunity for the community across the globe to come together, engage, interact and celebrate the latest research advances in embedded software and systems.

Embedded Systems Week (ESWEEK) is the premier event covering all aspects of hardware and software design for smart, intelligent and connected computing systems. By bringing together three leading conferences (CASES, CODES+ISSS and EMSOFT), a symposium (NOCS) and several workshops and tutorials, ESWEEK allows attendees to benefit from a wide range of topics covering the state of the art in embedded systems research and development. Embedded Systems Week (ESWEEK) is the premier event covering all aspects of hardware and software design for smart, intelligent and connected computing systems. By bringing together three leading conferences (CASES, CODES+ISSS and EMSOFT), a symposium (NOCS) and several workshops and tutorials, ESWEEK allows attendees to benefit from a wide range of topics covering the state of the art in embedded systems research and development.

Following the journal-integrated publication model for the three conferences (CASES, CODES+ISSS and EMSOFT), all regular papers presented are published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). To this end, ESWEEK-related journal submissions to TCAD followed a journal-style peer review process conducted in two stages with the opportunity of minor/major revisions before the final decision. In addition, the selected Work-in-Progress track papers are published in the ESWEEK Proceedings.

The technical program on Monday, Tuesday and Wednesday consists of 19 regular sessions from the three conferences. There is a strong emphasis on interaction in the virtual setting as all the accepted journal-track and Work-in-Progress track papers along with prerecorded video presentation for each paper are made available to the ESWEEK participants two weeks before the virtual event. The participants can discuss the papers with the authors through the virtual platform. During the actual virtual event, the live technical sessions will feature lightning talks for the journal-track papers followed by panel-style Q&A with the speakers in each session.

Highlights of the ESWEEK program are two distinguished keynote talks by prominent leaders in academia and industry, covering relevant trends for future embedded and cyberphysical systems and providing deep in sights into technology drivers. Professor John A. Rogers from the Northwestern University will introduce skin-like wireless wearables for continuous monitoring of physiological status with clinical-grade precision, designed for patient populations that range from premature babies in neonatal intensive care units to COVID-19 patients in the hospital and the home. Dr. Prith Banerjee, Chief Technology Officer at ANSYS, will discuss the challenges and opportunities of digital twins in various industries with a two-way information flow between the physical and virtual worlds using an IoT platform.
Welcome Messages

The conference program will feature the traditional panel on Wednesday focusing on 'Post COVID-19 Cyber Security-The Challenges and Solutions'. Top experts will share their views on this highly relevant topic.

The tutorials on Sunday precede the conferences and are an excellent opportunity to get in-depth knowledge in new trends and hot topics. There are four half-day, virtually presented tutorials, covering a wide scope, from domain-specific modeling language, open-source on-board software development to software-defined hardware design and simulation.

Thursday and Friday are the days for the symposium and workshops. Besides the NOCS (Networks on Chip) symposium, we have four workshops covering a wide range of important topics in embedded systems: RSP (Rapid System Prototyping), AAIEA (Accelerating Artificial Intelligence for Embedded Autonomy), HENP (Highly Efficient Neural Processing) and MSC (Memory and Storage Computing).

The organization of ESWEEK was only possible with the continuous support and help from the sponsors and many volunteers: The program chairs with their program committee members, the organizers of the workshops, tutorials and symposia, all members of the organization committee and last but not least, the virtual conference chair and the web chair—without their commitment and contributions this virtual event would not exist.

We are looking forward to seeing you virtually at the inspiring, interesting and interactive ESWEEK 2020!
Organizing Committee

General Chairs
Tulika Mitra, National University of Singapore, SG
Andreas Gerstlauer, University of Texas at Austin, US

Past Chair
Petru Eles, Linköping University, SE

Program Chairs
Partha Pande, Washington State University, US
Umit Ogras, Arizona State University, US
Roman Lysecky, University of Arizona, US

Organizational Chairs
A viral Shrivastava
Virtual Conference Chair
Arizona State University, US

Jürgen Teich
Awards Chair
Friedrich-Alexander University Erlangen-Nürnberg, DE

Andy Pimentel
Finance Chair
University of Amsterdam, NL

Andreas Herkersdorf
Industry Liaison Committee Chair
Technical University of Munich, DE

Geguang Pu
Industry Liaison Committee Chair
East China Normal University, CN

Dirk Ziegenbein
Industry Sessions Chair
Robert Bosch GmbH, DE

Yu Wang
Industry Sessions Chair
Tsinghua University, CN

Sri Parameswaran
Panel Chair
University of New South Wales, AU

Amit Singh
Publication Chair
University of Essex, UK

Lars Bauer
Publicity Chair
Karlsruhe Institute of Technology, DE

Shubham Rai
Social Media Chair
Technical University of Dresden, DE

Paul Bogdan
Special Sessions Chair
University of Southern California, US

Selma Saidi
Travel Grants Chair
Technical University of Dortmund, DE

Siddharth Garg
Tutorials Chair
New York University, US

Hoeseok Yang
Web Chair
Ajou University, KR

Patricia Derler
Workshop Chair
National Instruments, US
Program Committee (CASES)

Program Chairs
Partha Pratim Pande, Washington State University
Umit Ogras, Arizona State University

Members

Ali Akoglu, University of Arizona
Lars Bauer, KIT
Swarup Bhunia, University of Florida
Oliver Bringmann, University of Tuebingen / FZI
Luca Carloni, Columbia University
Jeronimo Castrillon, TU Dresden
Henri-Pierre Charles, CEA
Mainak Chaudhuri, IIT, Kanpur
Anup Das, Drexel University
Jana Doppa, Washington State University
Lide Duan, Alibaba DAMO Academy
Christophe Dubach, University of Edinburgh
William Fornaciari, Politecnico di Milano - DEIB
Amlan Ganguly, Rochester Institute of Technology
Puneet Gupta, UCLA
Yuko Hara-Azumi, Tokyo Institute of Technology
Joerg Henkel, KIT
Jinglong Hu, University of Pittsburgh
Paolo Ienne, EPFL
Hrishikesh Jayakumar, Qualcomm
Timothy Jones, University of Cambridge
Changhee Jung, Purdue University
Ramesh Karri, NYU
Ryan Kim, Colorado State University
Andreas Krall, TU Wien
Akash Kumar, TU Dresden
Jaemin Lee, Seoul National University

Chang-Gun Lee, Seoul National University
Mikko Lipasti, University of Wisconsin
Zhonghai Lu, KTH
Scott Mahlke, University of Michigan
Avinash Malik, University of Auckland
Michail Maniatakos, NYU
Pietro Mercati, Intel
Vijaykrishnan Narayanan, Penn State University
Rupesh Nasre, IIT, Chennai
Sri Parameswaran, UNSW
Anuj Pathania, National University of Singapore
Christian Pilato, Politecnico di Milano
Laura Pozzi, USI Lugano
Sai Manej Pudakotai Dinakar Rao, George Mason University
Sanghamitra Roy, Utah State University
Joshua San Miguel, University of Wisconsin
Aviral Shrivastava, Arizona State University
Amit Kumar Singh, University of Essex
Thorsten Struve, TU Dresden
Karthik Swaminathan, IBM
Hiroyuki Tomiyama, Ritsumeikan University
Jeffrey Vetter, Oakridge National Laboratory
Hao Wang, Higon R&D
Weng-Fai Wong, NUS
Shouyi Yin, Tsinghua University
Sungjoo Yoo, Seoul National University
Wei Zhang, HKUST

Info-5
Program Chairs
Roman Lysecky, University of Arizona
Jason Xue, City University of Hong Kong

Members
Houssam, Abbas, Oregon State University, USA
Tosiron Adegbija, University of Arizona
Siddharth Advani, Samsung Research
Mohammad Al Faruque, University of California, Irvine
Fatima M. Amvor, UMass Amherst
David Attene, École Polytechnique Fédérale de Lausanne (EPFL)
Lars Bauer, Karlsruhe Institute of Technology (KIT)
Giovanni Beltrame, Polytechnique Montreal
Christophe Bobda, University of Florida
Paul Bogdan, University of Southern California
Eli Bovnerzadeh, Univ. of California, Irvine
Oliver Bruegmann, University of Tuebingen / FZI
Yuan-Hao Chang, Academia Sinica
Wardl Chang, University of York
Yiran Chen, Duke University
Robert P. Dick, University of Michigan and Stryd
Rainer Doemer, University of California, Irvine
Jana Doppa, Washington State University
Nikil Dutt, University of California, Irvine
Petru Eles, Linkoping University
Xin Fang, Northeastern University
Fabrizio Ferrandi, Politecnico di Milano
Francesco Fummi, Università di Verona
Swaroop Ghoosh, Pennsylvania State University
Tony Givargis, University of California, Irvine
Dimitris Gizopoulos, University of Athens
Michael Gläß, Ulm University
Kees Goossens, Eindhoven University of Technology
Daniel Gross, University of Bremen/DFKI
Xiaochen Guo, Lehigh University
Seonho Ha, Seoul National University
Frank Hannig, Friedrich-Alexander University Erlangen-Nürnberg
Christian Haubelt, University of Rostock
Jörg Henkel, Karlsruhe Institute of Technology (KIT)
Houman Homayoun, George Mason University
Pi-Cheng Hsiu, Academic Sinica
Riley Jeyapaul, ARM Research
Ryan Kim, Colorado State University
Seontae Kim, KAIST
Fadi Kurdahi, University of California, Irvine
Luciano Lavagna, Politecnico di Torino
Sébastien Le Beux, Lyon Institute of Nanotechnology
Jenq-Kuen Lee, National Tsing Hua University
Kyoungwoo Lee, Yonsei University
Youn-Long Lin, National Tsing Hua University
Weichen Liu, Nanyang Technological University
Enrico Macii, Politecnico di Torino
Grant Martin, Cadence Design Systems
Hiroki Matsutani, Keio University
Nele Mentens, KU Leuven
Brett Meyer, McGill University
Prabhat Mishra, University of Florida
Wolfgang Mueller, University of Paderborn
Daniel Mueller-Gritschneder, Technical University of Munich
Mahdi Nikdast, Colorado State University
Umit Ogras, Arizona State University
Hyunok Oh, Hanyang University
Alex Ortolani, UC San Diego
Gianluca Palermo, Politecnico di Milano
Maurizio Palesi, University of Catania
Preeti Ranjan Panda, IIT Delhi
Partha Pratim Pande, Washington State University
Sudeep Pasricha, Colorado State University
Andy Pimentel, University of Amsterdam
Ilia Polian, University of Stuttgart
Louis Noel Pouchet, Ohio State University
Graziano Pravadelli, University of Verona
Amir M. Rahmani, University of California, Irvine
Ann Ramirez (Gordon-Ross), University of Florida
Francesco Regazzoni, ALaRI
Marco D. Santambrogio, Politecnico di Milano
Gunar Schirner, Northeastern University
Zhi Shao, The Chinese University of Hong Kong
Aviral Shrivastava, Arizona State University
Sandeep Shukla, Indian Institute of Technology Kanpur
Amit Kumar Singh, University of Essex
Todor Stefanov, Leiden University
Greg Stitt, University of Florida
Sander Stuijk, Eindhoven University of Technology
Fatemeh Tehranipoor, San Francisco State University
Jurgen Teich, University of Erlangen-Nuremberg
Ishan Thakkar, University of Kentucky
Hiroyuki Tomiyama, Ritsumeikan University
Frank Vahid, University of California, Riverside
Eugenio Villar, University of Cantabria
Chao Wang, University of Science and Technology of China
Jiang Xu, Hong Kong University of Science and Technology
Chengmo Yang, University of Delaware
Ming-Chang Yang, The Chinese University of Hong Kong
Haibo Zeng, Virginia Tech
Program Chairs

Timothy Bourke, Inria, France
Linh Thi Xuan Phan, University of Pennsylvania, USA

Members

Houssam Abbas, Oregon State University, USA
Tarek Abdelzaher, University of Illinois at Urbana Champaign, USA
Stanley Bak, SafeSky Analytics, USA
Ayca Balkan, Medtronic Inc, USA
Guillaume Baudart, IBM Watson, USA
Enrico Beni, University of Turin, Italy
Alessandro Biondi, Scuola Superiore Sant’Anna - Pisa, Italy
Sergiy Bogomolov, Newcastle University, UK
Borzoo Bonakdarpour, Iowa State University, USA
Björn Brandenburg, Max Planck Institute for Software Systems (MPI-SWS), Germany
Li-Pin Chang, National Chiao Tung University, Taiwan
Wanli Chang, University of York, UK
Thidapat Chantem, Virginia Tech, USA
David Cock, ETH Zurich, Switzerland
Thao Dang, CNRS, France
Pallab Dasgupta, IIT Kharagpur, India
Dionisio De Niz, CMU Software Engineering Institute, USA
André DeHon, University of Pennsylvania, USA
Patricia Derler, National Instruments, USA
Parasara Sridhar Duggirala, University of North Carolina at Chapel Hill, USA
Rolf Ernst, TU Braunschweig, Germany
Georgios Fainekos, Arizona State University, USA
Vinoth Ganapathy, Indian Institute of Science, Bangalore, India
Pierre-Loïc Garoche, Onera, Toulouse, France
Marc Geilen, Eindhoven University of Technology, The Netherlands
Gregor Goesslser, Inria, France
Kees Goossens, Eindhoven University of Technology, The Netherlands
Nan Guan, The Hong Kong Polytechnic University
Zhishan Guo, University of Central Florida, USA
Ichiro Hasuo, National Institute of Informatics, Japan
Jean-Baptiste Jeannin, University of Michigan, USA
Swarun Kumar, Carnegie Mellon University, USA
Shan Lin, Stonybrook University
Srikanta Mancuso, Boston University, USA
Matthieu Moy, Université Claude Bernard Lyon, France
Sam H. Noh, Ulsan National Institute of Science and Technology (UNIST), South Korea
Necmiye Ozay, University of Michigan, USA
Claire Pagetti, Onera / ENSEEIHT, France
Gabriel Parmer, George Washington University, USA
Marc Pouzet, École normale supérieure, France
Pavithra Prabhakar, Kansas State University, USA
Sylvie Putot, École polytechnique, France
S.S. Ramesh, General Motors, USA
Abhik Roychoudhury, National University of Singapore, Singapore
Indranil Saha, IIT Kharagpur, India
Wolfgang Schröder-Preikschat, Friedrich-Alexander University Erlangen-Nürnberg, Germany
Donatella Sciuto, Polytechnic University of Milan, Italy
Lothar Thiele, ETH Zürich, Switzerland
Marcus Volp, University of Luxembourg, Luxembourg
Bryan Ward, MIT Lincoln Laboratory, USA
Gera Weiss, Ben Gurion University of the Negev, Israel
Bai Xue, State Key Laboratory of Computer Science, Institute of Software, Chinese Academy of Sciences, China
Jason Xue, City University of Hong Kong
Naijun Zhan, State Key Laboratory of Computer Science, Institute of Software, Chinese Academy of Sciences, China

WiP Committee

Mihail Asavoae, CEA List, France
Unmesh Dutta Bordoloi, General Motors, USA
Arvind Easwaran, Nanyang Technological University, Singapore
Petru Eles, Linkoping University, Sweden
Fanxin Kong, Syracuse University, USA
Vuk Lesi, Intel Labs, USA
Chung Wei Lin, National Taiwan University, Taiwan
Mitra Nasri, Eindhoven University of Technology, Netherlands
Oleg Sokolsky, University of Pennsylvania, USA
Adam Kostrzewa  
Adrien Guatto  
Akarsh Prabhakara  
Akhiisa Yamada  
Akshay Gadre  
Akshay Mambakam  
Alain Girault  
Ali Ozdagli  
Aline Resahani  
Andreas Biri  
Antonio Bruno da Costa  
Anway Muckherjee  
Aritra Hazra  
Arpan Gujarati  
Arun Adiththan  
Ashikamedh Bhuiyan  
Asha Farhangi  
Atul Bansal  
Bassel El Mabsout  
Benedict Herzig  
Bomseok Nam  
Bohua Zhan  
Borislaw Nikolic  
Britt Gangopadhyay  
Carlos Barreto  
Claire Maiza  
Daniel Casini  
Daniel Lundén  
Denis Hoomaert  
Dharmesh Tarapore  
Dana Zhang  
Dimitrios Boursinos  
Dung Tran  
Elias Castegren  
Federico Reghenzani  
Feiyang Cai  
Frederic Boniol  
Georg von der Bruggen  
Glen Chou  
Golsana Ghaemi  
Guillaume Salagnac  
Hamza Boubouh  
Haojian Jin  
Hoang-Dung Tran  
Ismail Lahkim-Bennani  
Jean-Louis Colaço  
Jiang Bian  
Jiani Li  
Jingxuan Wang  
Johannes Schlattow  
Joseph Devietti  
Kai Gemlau  
Kostiantyn Potomkin  
Kwesi Rutledge  
Lelio Brun  
Linnea Ingmar  
Liren Yang  
Marco Maida  
Marco Perronet  
Mauricio Chimento  
Md Sanzid Bin Hossain  
Mischa Moestl  
Mischa Mostl  
Naomi Stricker  
Nathanael Sensfelder  
Nikolaos Kekatos  
Oscar Eriksson  
Pascal Fradet  
Pascal Raymond  
Paulius Stankaitis  
Paul Rouse  
Peter Ulbrich  
Peter Waeremamm  
Phillip Raffeck  
Pierre-Julien Chaine  
Prakash M. Peranandam  
Pranav Ashok  
Pratham Oza  
Rami Debouk  
Ratan Lal  
Roman Trueb  
Sadegh Soudjani  
Saeid Dehnavi  
Saranya Natarajan  
Sergey Bohzko  
Shahin Roozkhoosh  
Shakibi Yaghoubi  
Shayan Tahatabaei  
Simon Schuster  
Stefan Draskovic  
Stefan Klikovits  
Stefan Reif  
Sudharsan Vaidhun  
Sadipa Mandal  
Info-10
Takamasa Okudono
Tanmaya Mishra
Thawra Kadeed
Thomas Mari
Timo Hoerig
Tim Rheinfels
Tobias Blass
Túlio Pascoal
Vaibhav Singh
Viktor Palmkvist

Waseem Abbas
Weijiang Kong
Xiaoyi Zhang
Yinghe Han
Youcef Bouchebaba
Zexiang Liu
Zhan Gao
Zheng Dong
Zhongnan Qu
Keynote Talks
Date/Time: September 21, 2020 (Monday)

Skin-Like Wireless Wearables-From Premature Babies in the NICU to Patients with COVID-19

Professor John A. Rogers
Northwestern University; Simpson/Querrey Institute McCormick School of Engineering; Weinberg College of Arts and Sciences and Feinberg School of Medicine, IL , USA

Biography

Professor John A. Rogers
Northwestern University;
Simpson/Querrey Institute McCormick School of Engineering;
Weinberg College of Arts and Sciences and Feinberg School of Medicine IL, USA.

John A. Rogers is the Simpson/Querrey Professor of Materials Science and Engineering, Biomedical Engineering and Medicine at Northwestern University, where he is also Director of the Institute for Bioelectronics. He has published more than 750 papers, he is a co-inventor on more than 100 patents and he has co-founded several successful technology companies. His research has been recognized by many awards, including a MacArthur Fellowship (2009), the Lemelson-MIT Prize (2011) and the Benjamin Franklin Medal (2019). He is a member of the National Academy of Engineering, the National Academy of Sciences, the National Academy of Medicine and the American Academy of Arts and Sciences.

Abstract

Recent global events are reshaping the geopolitical and socio-economic landscape in ways that will likely alter research priorities for at least a generation - a broad consensus is that long-term solutions to the underlying societal challenges will only occur through innovative technologies and advanced medicines, as life-saving diagnostics, digital biosensors, therapeutics and preventatives. This talk will outline work that intersects with essential unmet needs in this broader context, specifically in the form of skin-like wireless wearables for continuous monitoring of physiological status with clinical-grade precision. The focus is on foundational ideas in materials, design and manufacturing, with examples of devices designed for patient populations that range from premature babies in neonatal intensive care units to COVID-19 patients in the hospital and the home - both deployed locally within the medical complex here in Chicago and globally in clinics across lower and middle income countries in Africa and Central America.
Date/Time: September 22, 2020 (Tuesday)

Digital Twins: Challenges and Opportunities in Various Industries

Dr. Prith Banerjee
Chief Technology Officer, ANSYS, PA, USA

Biography

Prith Banerjee is Chief Technology Officer at ANSYS, a leader in engineering simulation. In this role, he leads the evolution of ANSYS' technology and champions the company’s next phase of innovation and growth. Prior to that, he was Executive Vice President and Chief Technology Officer of Schneider Electric. Formerly, he was Managing Director of Global Technology R&D at Accenture. Earlier, he was Chief Technology Officer and Executive Vice President of ABB. Earlier, he was Senior Vice president of Research and Director of HP Labs. Formerly, he was Dean of the College of Engineering at the University of Illinois at Chicago. Formerly he was the Walter P. Murphy Professor and Chairman of ECE at Northwestern University. Prior to that, he was professor of ECE at the University of Illinois. In 2000, he was Founding CEO of AccelChip which was sold to Xilinx Inc. in 2006. During 2005-2011, he was Founder, Chairman and Chief Scientist of BINACHIP. His research interests are in electronic design automation, and parallel computing, and he is the author of about 350 research papers. He has also supervised 37 Ph.D. students. Banerjee currently serves on the Board of Directors of Cubic Corporation and Software Motor Company. In the past, he has served on Boards for Cray, Inc., the Anita Borg Institute, the Computer Science Board of the National Academy of Engineering and the Technical Advisory Boards of Ambit, Atrenta, Calypto, and Cypress. He was listed in the FastCompany list of 100 top business leaders in 2009. He is a Fellow of the AAAS, ACM and IEEE and a recipient of the 1996 ASEE Terman Award and the 1987 NSF Presidential Young Investigator Award. He received a B.Tech. (President’s Gold Medalist) in electronics engineering from the Indian Institute of Technology, Kharagpur, and an M.S. and Ph.D. in electrical engineering from the University of Illinois, Urbana.

Abstract

Various industries such as Manufacturing, Energy and Utilities, Automotive, Aerospace and Defense, Logistics and Transportation, and Building Management, have proposed the use of Digital Twins to aid the Design, Analysis, Build, Manufacturing and Operations phases of asset-intensive industries. Digital Twins have a physical asset, a virtual asset (a simulation model of the asset), and a two-way information flow between the physical and virtual worlds using an IOT platform. While most companies use data-based analytics and machine learning to build Digital Twins, they require lots of training data and the accuracy is limited to the observed data. Some industries have started using physics based simulation to build digital twins and while these approaches are accurate they require long computation times to deploy. Most recently, companies are using Hybrid approaches combining data-based analytics and physics-based approaches to build these digital twins that are very accurate and require less training data, and drive high operational efficiency of assets and process industries and manufacturing plants. In this talk we will discuss the challenges and opportunities of digital twins in various industries and the latest research approaches.
Panel
Date/Time: September 23, 2020 (Wednesday) / 10:00 – 11:00 hrs

Post COVID-19 Cyber Security: The Challenges and Solutions
Prof. Sri Parameswaran

Panellists

Prof. Richard Buckland
Director of First Year Experience of UNSW, Professor in CyberCrime Cyberwar and Cyberterror at the School of Computer Science and Engineering University of New South Wales, Australia

Prof. Farinaz Koushanfar
Professor & Henry Booker Faculty Scholar Electrical and Computer Engineering (ECE) Department University of California San Diego (UCSD) USA

Prof. Nasir Memon
Vice Dean for Academics and Student Affairs and a Professor Computer Science and Engineering The New York University Tandon School of Engineering USA

Prof. Ingrid Verbauwhede
Research group COSIC, KU Leuven, ESAT/COSIC Heverlee, België
Tutorials
**Date/Time:** September 20, 2020 (Sunday) / 09:00 – 01:00 hrs

Half-Day Tutorial with Hands-on Practical Training

**Creating Domain-Specific Modeling Languages: Hands-on**

Dr. Juha-Pekka Tolvanen and Dr. Steven Kelly

---

**Biography**

**Dr. Juha-Pekka Tolvanen** is CEO of MetaCase. He has been involved in domain-specific languages and tools since 1991 and acted as a consultant world-wide on their use. Juha-Pekka has co-authored a book (Domain-Specific Modeling, Wiley 2008) and over 80 articles in software development magazines and conferences. Juha-Pekka holds a Ph.D. in computer science.

**Dr. Steven Kelly** is CTO of MetaCase and co-founder of the DSM Forum. He has over twenty years of experience of tool building and consultancy in Domain-Specific Modeling. As architect and lead developer of MetaEdit+, he has seen it win or be a finalist in awards from SD Times, Byte, and Jolt Productivity. He has co-authored a book and published over 50 articles in journals and conferences. Steven is a member of IASA and on the editorial board of the Journal of Database Management.

---

**Description**

A horrible lie exists in our industry today: it says that defining a graphical domain-specific languages (DSLs) is difficult and time-consuming. In this tutorial, we will lay bare this fallacy and demonstrate how simple and quick it is to create domain-specific languages and their generators. Using a hands-on approach you will define several modeling languages and generators within a few hours, learning principles and best practices proven in industrial experience.

The tutorial teaches practical, repeatable steps to invent and implement DSL. The language definition process reveals the characteristics of DSLs that enable generating working code from models:

- DSL is based on the concepts of problem domain rather than code
- Scope of the language narrowed down to a particular domain
- Language minimizes the effort needed to create, update and check the models
- Experience on using at least one modeling tool is required. Experience on language creation is not required.
Tutorial

**Date/Time:** September 20, 2020 (Sunday) / 09:00 – 01:00 hrs

(Half-Day Tutorial with Hands-on Practical Training)

**Software-Defined Hardware: Digital Design with Chisel**

Prof. Martin Schoeberl

---

**Biography**

**Martin Schoeberl** received his PhD from the Vienna University of Technology in 2005. From 2005 to 2010 he has been Assistant Professor at the Institute of Computer Engineering. He is now Associate Professor at the Technical University of Denmark. His research interest is on hard real-time systems, time-predictable computer architecture, and real-time Java. Martin Schoeberl has been involved in a number of national and international research projects: JEOPARD, CJ4ES, T-CREST, RTEMP, the TACLe COST action, and PREDICT. He has been the technical lead of the EC funded project T-CREST. He has more than 100 publications in peer reviewed journals, conferences, and books.

Martin has been four times at UC Berkeley on 3-4 months research stays, where he has picked up Chisel and was in close contact with the developers of Chisel. He lead the research project T-CREST where most of the components have been written in Chisel.

Martin has published the book "Digital Design with Chisel", already in the 2nd edition, which is available in open source.

---

**Description**

To develop future more complex digital circuits in less time we need a better hardware description language than VHDL or Verilog. Chisel is a hardware construction language intended to speed up the development of digital hardware and hardware generators.

Chisel is a hardware construction language implemented as a domain-specific language in Scala. Therefore, the full power of a modern programming language is available to describe hardware and, more important, hardware generators. Chisel has been developed at UC Berkeley and successfully used for several tape outs of RISC-V by UC Berkeley students and a chip for a tensor processing unit by Google. Here at the Technical University of Denmark we use Chisel in the T-CREST project and in teaching digital electronics and advanced computer architecture.

In this tutorial we will give an overview of Chisel to describe circuits, how to use the Chisel tester functionality to test and simulate digital circuits, present how to synthesize circuits for an FPGA, and present advanced functionality of Chisel for the description of circuit generators.

The aim of the course is to get a basic understanding of a modern hardware description language and be able to describe simple circuits in Chisel. This course will give a basis to explore more advanced concepts of circuit generators written in Chisel/Scala. The intended audience is hardware designers with some background in VHDL or Verilog, but Chisel is also a good first hardware language for software programmers entering into hardware design (e.g., porting software algorithms to FPGAs for speedup).
Out-of-Order Parallel Simulation of SystemC Models using the RISC Framework

Prof. Rainer Dömer

Description

The simulation of large SystemC models is slow due to the sequential nature of traditional simulators, such as the Accellera proof-of-concept reference implementation. Parallel Discrete Event Simulation (PDES) offers an order of magnitude speedup, but incurs obstacles due to the cooperative multi-threading semantics of IEEE SystemC.

This tutorial introduces and practices the Recoding Infrastructure for SystemC (RISC) framework which enables aggressive automatic parallelization of SystemC simulation by use of out-of-order PDES which can achieve two orders of magnitude speedup. RISC also features advanced thread-aware static analysis of SystemC models using a dedicated compiler and segment graph data structure that allow deep insight into the potential parallelization of design models at hand.

Introduction to Out-of-Order Parallel Discrete Event Simulation
Overcoming the obstacles of IEEE SystemC Semantics
RISC: Recoding Infrastructure for SystemC
Hands-on Practical Training with RISC Compiler and Simulator
Hands-on Practical Analysis of Parallel Potential of SystemC Models
Tutorial

Date/Time: September 20, 2020 (Sunday) / 09:00 – 01:00 hrs

(Pre-recorded Presentations with 1 hour Live Q&A)

Tasking Framework: An open-source software development library for on-board software systems

Dr. Zain A. H. Hammadeh and Dr. Olaf Maibaum

Biography

Zain A. H. Hammadeh is a research scientist at the German Aerospace Center (DLR). In 2019, he received his Ph.D. degree (Dr.-Ing.) in real-time systems from TU Braunschweig, Germany with Prof. Rolf Ernst. Since Feb. 2019 he joined the Institute for Software Technology as a research scientist.

Olaf Maibaum is a research scientist at the German Aerospace Center (DLR) since 2000. He was involved at DLR as software engineer for the on-board control software in several space projects, e.g. the attitude control systems of the BIRD, TET-1 and EU CROPIS small satellites. He received his Ph.D degree (Dr. rer. nat.) at the Carl von Ossietzky University in Oldenburg at the institute of Operating Systems and Distributed Systems in the year 2002 on the topic of static analysis of assembler code to determine the WCET in embedded real time software.

Description

Tasking Framework is a C++ software development library and an event-driven multithreading execution platform. It is developed by the Institute for Software Technology, German Aerospace Center (DLR). Tasking Framework is dedicated to improve the reusability in developing embedded software systems and to reconcile the embedded software with model-driven software development. It can be used to develop, but not dedicated for, critical as well as non-critical embedded software on single-core as well as parallel architectures. Tasking Framework gives software developers the ability to implement their applications as task graphs with arbitrary activation patterns (periodic, aperiodic and sporadic) using a set of abstract classes with virtual methods. It is compatible with the POSIX-based operating systems, mainly Linux and RTEMS. The Tasking Framework was successfully used in, for instance, the attitude orbit control system of a satellite, the experiment control system on a sounding rocket, and in a lunar navigation system.

In this tutorial, we will present the main features of Tasking Framework, how to get it, use cases, and development process.
## Session 1A: CASES - Memory Technologies

### Date/Time
September 21, 2020 (Monday) / 11:00 — 11:45 hrs

### Moderator
Sudeep Pasricha, Colorado State University, USA

### Description
Memory has been a key component of various computing platforms starting from mobile devices to high-performance computing (HPC) systems. This session presents papers showcasing recent advances on memory technologies.

### Papers

#### Hardware Memory Management for Future Mobile Hybrid Memory Systems
Fei Wen, Texas A&M University  
Mian Qin, Texas A&M University  
Paul Gratz, Texas A&M University  
Narasimha Reddy, Texas A&M University

#### Patch-based Data Management for Dual-copy Buffers in RAID-enabled SSDs
Jun Li, Southwest University of China  
Zhbing Sha, Southwest University of China  
Zhigang Cai, Southwest University of China  
Francois Trahay, Telecom SudParis, France  
Jianwei Liao, Southwest University of China

#### Polyhedral Compilation for Racetrack Memories
Asif Ali Khan, TU Dresden  
Hauke Mewes, TU Dresden  
Tobias Grosser, ETH Zurich  
Torsten Hoefler, ETH Zurich  
Jeronimo Castrillon, TU Dresden

#### AXFTL: Exploiting Error Tolerance for Extending Lifetime of NAND Flash Storage
Yongwoo Lee, University of Wisconsin-Madison  
Jaehyun Park, University of Ulsan  
Junhee Ryu, SK Hynix  
Youngyuan Kim, University of Wisconsin-Madison

#### Optimization of Intercache Traffic Entanglement in Tagless Caches With Tiling Opportunities
S R Swamy Saranam Chongala, Indian Institute of Technology Madras  
Sumitha George, PSU  
Hariram Thirucherai Govind, PSU  
Jagadish Kotra, AMD  
Madhu Mutyam, IIT Madras  
John, Jack Sampson, Penn State  
Mahmut Kandemir, PSU  
Vijaykrishnan Narayanan, Penn State University
**Session 1B: CODES+ISSS-Neural Network and Acceleration**

**Date/Time:** September 21, 2020 (Monday) / 11:00 — 11:45 hrs

**Moderator:** Yuan-Hao Chang, Academia Sinica, Taiwan

**Description:** Deep learning and neural networks are increasingly becoming a key component of embedded systems across numerous application domains. This session explores both the design of energy-efficient and high-performance neural network accelerators and design space exploration methods to assist in designing those accelerators.

---

**Everything Leaves Footprints: Hardware Accelerated Intermittent Deep Inference**

Chih-Kai Kang, Academia Sinica
Hashan Roshantha Mendis, Academia Sinica
Chun-Han Lin, National Taiwan Normal University
Ming-Syan Chen, National Taiwan University
Pi-Cheng Hsiu, Academia Sinica

**FSA: A Fine-Grained Systolic Accelerator for Sparse CNNs**

Fanrong Li, Institute of Automation, CAS
Gang Li, Institute of Automation, CAS
Zitao Mo, Institute of Automation, CAS
Xiangyu He, Institute of Automation, CAS
Jian Cheng, Institute of Automation, CAS

**StereoEngine: An FPGA-based Accelerator for Real-Time High-quality Stereo Estimation with Binary Neural Network**

Gang Chen, Sun Yat-sen University
Yehua Ling, Sun Yat-sen University
Tao He, Northeastern University
Haitao Meng, Northeastern University
Shengyu He, Northeastern University
Yu Zhang, Sun Yat-sen University
Kai Huang, Sun Yat-sen University

**SuperSlash: A Unified Design Space Exploration and Model Compression Methodology for Design of Deep Learning Accelerators With Reduced Off-Chip Memory Access Volume**

Hazoor Ahmad, Information Technology University
Tabasheer Arif, ITU
Muhammad Abdullah Hanif, Institute of Computer Engineering, Vienna University of Technology
Rehan Hafiz, ITU
Muhammad Shafique, Vienna University of Technology, TU Wien

**WinoNN: Optimizing FPGA-Based Convolutional Neural Network Accelerators Using Sparse Winograd Algorithm**

Xuan Wang, University of Science and Technology of China
Chao Wang, University of Science and Technology of China
Jing Cao, University of Science and Technology of China
Lei Gong, University of Science and Technology of China
Xuehai Zhou, University of Science and Technology of China
Session 1C: EMSOFT - Real-Time Scheduling
Date/Time: September 21, 2020 (Monday) / 11:00 — 11:45 hrs
Moderator: Tarek Abdelzaher, University of Illinois at Urbana Champaign, USA
Description: Scheduling algorithms and analyses with a focus on real-time and energy.

Suspension-Aware Earliest-Deadline-First Scheduling Analysis
Mario Guenzel, TU Dortmund University
Georg von der Brüggen, Max Planck Institute for Software Systems (MPI-SWS)
Jian-Jia Chen, TU Dortmund

Static Scheduling of Moldable Streaming Tasks with Task Fusion for Parallel Systems with DVFS
Christoph Kessler, Linköping University
Sebastian Litzinger, FernUniversität in Hagen
Joerg Keller, FernUniversität in Hagen

Efficient Feasibility Analysis for Graph-based Real-Time Task Systems
Jinghao Sun, Dalian University of Technology
Rongxiao Shi, Northeastern University
Kexuan Wang, Northeastern University
Nan Guan, The Hong Kong Polytechnic University
Zhishan Guo, University of Central Florida

Precedence-aware Automated Competitive Analysis of Real-Time Scheduling
Krishnendu Chatterjee, IST Austria
Andreas Pavlogiannis, Aarhus University
Nico Schurmann, Vienna University of Technology
Ulrich Schmid, Vienna University of Technology

Dynamic DAG Scheduling on Multiprocessor Systems: Reliability, Energy, and Makespan
Jing Huang, Hunan University
Renfa Li, Hunan University
Xun Jiao, Villanova University
Yu Jiang, Tsinghua University
Wanli Chang, University of York
<table>
<thead>
<tr>
<th>Session</th>
<th>2A: CASES- Energy-efficient ML for IoT and Edge Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Date/Time</td>
<td>September 21, 2020 (Monday) / 11:45 — 12:30 hrs</td>
</tr>
<tr>
<td>Moderator</td>
<td>Ryan Kim, Colorado State University, USA</td>
</tr>
<tr>
<td>Description</td>
<td>Advances in Machine Learning (ML) algorithms are key for the successful deployment of IoT and edge devices. This session focuses on application of ML algorithms in resource constraint environments.</td>
</tr>
</tbody>
</table>

**Fusion-Catalyzed Pruning for Optimizing Deep Learning on Intelligent Edge Devices**

Guangli Li, Institute of Computing Technology, Chinese Academy of Sciences
Xiu Ma, Jilin University
Xueying Wang, Institute of Computing Technology, Chinese Academy of Sciences
Lei Liu, Institute of Computing Technology, Chinese Academy of Sciences
Jingling Xue, UNSW Sydney
Xiaobing Feng, Institute of Computing Technology, Chinese Academy of Sciences

**Efficient Scheduling of Irregular Network Structures on CNN Accelerators**

Shixuan Zheng, Tsinghua University
Xianjue Zhang, Tsinghua University
Daoqi Ou, Tsinghua University
Shibin Tang, TsingMicro Tech. Ltd.
Leibo Liu, Tsinghua University
Shaojun Wei, Tsinghua University
Shouyi Yin, Tsinghua University

**FSPiNN: An Optimization Framework for Memory-Efficient and Energy-Efficient Spiking Neural Networks**

Rachmad Vidyawicaksana Putra, Technische Universität Wien
Muhammad Shafique, Vienna University of Technology
TU Wien

**Analyzing Deep Learning for Time-Series Data through Adversarial Lens in Mobile and IoT Applications**

Taha Belkhouja, Washington State University
Jana Doppa, Washington State University

**MacLeR: Machine Learning-Based Runtime Hardware Trojan Detection in Resource-Constrained IoT Edge Devices**

Faiq Khalid, Technische Universität Wien
Syed Rafay Hasan, Tennessee Techné University
Sara Zia, NUST SEECS
Osman Hasan, NUST
Falah Awwad, United Arab Emirates University
Muhammad Shafique, Vienna University of Technology
TU Wien
Session 2B: CODES+ISSS — Multicore and Approximate Architectures
Date/Time September 21, 2020 (Monday) / 11:45 — 12:30 hrs
Moderator Liang Shi, East China Normal University, China
Description High-performance and energy-efficient multicore architectures are widely utilized within modern embedded systems. This session presents novel methods for approximate computing, approximate communication, time-predictable memory architectures and more accurate power estimation methods.

Learning-Based Quality Management for Approximate Communication in Network-on-Chips
Yuechen Chen, The George Washington University
Ahmed Louri, The George Washington University

Aggressive Fine-Grained Power Gating of NoC Buffers
Yibo Wu, Tsinghua University
Leibo Liu, Tsinghua University
Liang Wang, Tsinghua University
Xiaohang Wang, South China University of Technology
Jie Han, University of Alberta
Chenchen Deng, Tsinghua University
Shaojun Wei, Tsinghua University

Meshed Bluetree: Time-Predictable Multimemory Interconnect for Multicore Architectures
Haitong Wang, University of York
Neil Audsley, University of York
X. Sharon Hu, University of Notre Dame
Wanli Chang, University of York

Risk-5: Controlled approximations for RISC-V
Isaías Bittencourt Felzmann, University of Campinas
João Fabricio Filho, Unicamp/UFPR
Lucas Warner, Unicamp

A Lightweight Nonlinear Methodology to Accurately Model Multicore Processor Power
Mark Sagi, TU Munich
Nguyen Anh Vu Doan, Technical University of Munich
Martin Rapp, Karlsruhe Institute of Technology
Thomas Wild, Technical University of Munich
Joerg Herskel, JF
Andreas Herkersdorf, TU München
Session 2C:EMSOFT — Energy Aware Applications and Techniques

Date/Time September 21, 2020 (Monday) / 11:45 — 12:30 hrs

Moderator Lothar Thiele, ETH Zürich, Switzerland

Description Techniques and applications with a focus on optimizing battery performance and energy use.

**LATICS: A Low-overhead Adaptive Task-based Intermittent Computing System**
Songran Liu, Northeastern University
Wei Zhang, The Hong Kong Polytechnic University
Mingsong Lv, Northeastern University
Qiulin Chen, Huawei Technologies Co., Ltd.
Nan Guan, The Hong Kong Polytechnic University

**Managing Fleets of LEO Satellites: Nonlinear, Optimal, Efficient, Scalable, Usable, and Robust**
Gregory Stock, Saarland University
Juan Fraire, Saarland University
Tobias Mömke, Saarland University
Holger Hermanns, Saarland University
Fakhri Babayev, GomSpace A/S
Eduardo Cruz, GomSpace A/S

**Optimizing Discharge Efficiency of Reconfigurable Battery With Deep Reinforcement Learning**
Seunghyeok Jeon, Yonsei University
Jiwon Kim, Yonsei University
Junick Ahn, Yonsei University
Hojung Cha, Yonsei University

**Opttrone: Maximizing Performance and Energy Resources of Drone Batteries**
Jiwon Kim, Yonsei University
Yonghun Choi, Yonsei University
Seunghyeok Jeon, Yonsei University
Jaeyun Kang, Yonsei University
Hojung Cha, Yonsei University

**Optimizing Energy in Non-preemptive Mixed-Criticality Scheduling by Exploiting Probabilistic Information**
Ashikahmed Bhuiyan, University of Central Florida
Federico Reghenzani, Politecnico di Milano
William Fornaciari, Politecnico di Milano
Zhitian Guo, University of Central Florida
ESWEEK 2020 — Technical Programme

Session 3A: CASES — Processor Architecture
Date/Time September 22, 2020 (Tuesday) / 11:00 — 11:45 hrs
Moderator Ganapati Bhat, Washington State University, USA

Description

Heterogeneous processors have been at the heart of the state-of-the-art many-core architectures. This session presents latest scheduling, run-time management and optimization of processor architecture under emerging workloads.

Fast and Correct Load-Link/Store-Conditional Instruction Handling in DBT Systems
Martin Kristien, University of Edinburgh
Tom Spink, University of Edinburgh
Brian Campbell, University of Edinburgh
Susmit Sarkar, University of St. Andrews
Ian Stark, University of Edinburgh
Bjorn Franke, University of Edinburgh
Igor Bohm, Synopsys Inc.
Nigel Topham, University of Edinburgh

VisSched: An Auction-Based Scheduler for Vision Workloads on Heterogeneous Processors
Diksha Moolchandani, IIT Delhi
Anshul Kumar, IIT Delhi
José F. Martinez, Cornell University
Smruti R. Sarangi, IIT Delhi

Dynamic Power and Energy Management for NCFET-based Processors
Sami Salamin, Karlsruhe Institute of Technology
Martin Rapp, Karlsruhe Institute of Technology
Joerg Henkel, KIT
Andreas Gerstlauer, The University of Texas at Austin
Hussam Amrouch, Karlsruhe Institute of Technology

FINDER: Find Efficient Parallel Instructions for ASIPs to Improve Performance of Large Applications
Vikkitharan Gnanasambandam, UNSW
Jorgen Peddersen, UNSW
Roshan Ragel, University of Peradeniya
Sri Parameswaran, UNSW

NPU Thermal Management
Hussam Amrouch, Karlsruhe Institute of Technology
Georgios Zervakis, Karlsruhe Institute of Technology
Sami Salamin, Karlsruhe Institute of Technology
Hammam Kattan, Karlsruhe Institute of Technology
Iraklis Anagnostopoulos, Southern Illinois University Carbondale
Joerg Henkel, KIT
Session 3B: CODES+ISSS — HLS and System Design

Date/Time September 22, 2020 (Tuesday) / 11:00 — 11:45 hrs
Moderator Ann Gordon-Ross, University of Florida, USA

Description The increasing complexity of embedded systems demands efficient system design methodologies to assist designers in optimizing and secure these systems. This session presents high-level synthesis and system-level design methods that can optimize design for different underlying architectures.

Tensor Optimization for High-level Synthesis Design Flows
Marco Siracusa, Politecnico di Milano
Fabrizio Ferrandi, Politecnico di Milano

AnyHLS: High-Level Synthesis with Partial Evaluation
M. Akif Özkan, Friedrich-Alexander-Universität Erlangen-Nürnberg, FAU
Arsène Pérard-Gayot, Saarland University
Richard Membarth, Saarland University
Philipp Slusallek, DFKI & Saarland University
Roland Leißa, Saarland University
Sebastian Hack, Saarland University
Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg, FAU
Frank Hannig, Friedrich-Alexander University Erlangen-Nürnberg, FAU

Standing on the Shoulders of Giants: Hardware and Neural Architecture Co-Search with Hot Start
Weiswen Jiang, University of Notre Dame
Lei Yang, University of Notre Dame
Sakyasingha Dasgupta, Edgecortix Inc.
Jingtong Hu, University of Pittsburgh
Yiyu Shi, University of Notre Dame

MeXT-SE: A Design Tool to Transparently Generate Secure MPSoC
Md Jubaer Hossain Pantho, University of Florida
Christophe Bobda, University of Florida
Safety Verification for Random Ordinary Differential Equations
Bai Xue, Institute of Software, Chinese Academy of Sciences
Naijun Zhan, Institute of Software, Chinese Academy of Sciences
Sergiy Bogomolov, Newcastle University
Bican Xia, School of Mathematical Sciences, Peking University

Reachability analysis of linear hybrid systems via block decomposition
Sergiy Bogomolov, Newcastle University
Marcelo Forets, Universidad de la Republica
Goran Frehse, University of Grenoble Alpes — Verimag
Kostiantyn Potomkin, Newcastle University
Christian Schilling, IST Austria

Hybrid System Falsification under (In)equality Constraints via Search Space Transformation
Zhenya Zhang, National Institute of Informatics
Paolo Arcaini, National Institute of Informatics
Ichiro Hasuo, National Institute of Informatics

Divide and Slide: Layer-Wise Refinement for Output Range Analysis of Deep Neural Networks
Chao Huang, Northwestern University
Jiameng Fan, Boston University
Xin Chen, University of Dayton
Wenchao Li, Boston University
Qi Zhu, Northwestern University

Pruning Deep Reinforcement Learning for Dual User Experience and Storage Lifetime Improvement on Mobile Devices
Chao Wu, City University of Hong Kong
Yu Fei Cui, City University of Hong Kong
Cheng Ji, Nanjing University of Science and Technology
Tei-Wei Kuo, City University of Hong Kong
Jason Xue, City University of Hong Kong
Resource management is essential to improve performance and energy-efficiency of processors. This session presents papers addressing high level synthesis, memory management and security challenges in processor architectures.

Toward Speculative Loop Pipelining for High-Level Synthesis
Steven Derrien, University of Rennes 1/IRISA
Thibaut Marty, Univ Rennes, Inria, CNRS, IRISA
Simone Rokicki, Irisa
Tomofumi Yuki, INRIA

Leveraging Prior Knowledge for Effective Design-Space Exploration in High-Level Synthesis
Lorenzo Ferretti, Universit della Svizzera italiana
Jihye Kwon, Columbia University
Giovanni Arsaleni, USI Lugano
Giuseppe Di Guglielmo, Columbia University
Luca Carioni, Columbia University
Laura Pozzi, USI Lugano

Maskara: Compilation of a Masking Countermeasure With Optimized Polynomial Interpolation
Nicolas Belleville, Univ Grenoble Alpes, CEA, List, F-38000 Grenoble
Damien Couroussé, Univ Grenoble Alpes, CEA, LIST, F-38000 Grenoble, France
Karine Heydemann, Sorbonne Université, CNRS, LIP6, F-75005 Paris, France
Quentin Meunier, Sorbonne Université, CNRS, LIP6, F-75005 Paris, France
Inès Ben El Ouahma, Sorbonne Université, CNRS, LIP6, F-75005 Paris, France

Boosting User Experience via Foreground-Aware Cache Management in UFS Mobile Devices
Chao Wu, City University of Hong Kong
Qiao Li, City University of Hong Kong
Cheng Ji, Nanjing University of Science and Technology
Tei Wei Kuo, City University of Hong Kong
Jason Xue, City University of Hong Kong

Combating Enhanced Thermal Covert Channel in Multi-/Many-core Systems with Channel-aware Jamming
Jiachen Wang, South China University of Technology
Xiaohang Wang, South China University of Technology
Yingtao Jiang, University of Nevada, Las Vegas
Amit Kumar Singh, University of Essex
Letian Huang, University of Electronic Science and Technology of China
Mei Yang, University of Nevada, Las Vegas
ABCFI: Fast and Lightweight Fine-Grained Hardware-Assisted Control-Flow Integrity
Jinfeng Li, Institute of Information Engineering, Chinese Academy of Sciences, School of Cyber Security, University of Chinese Academy of Sciences
Liwei Chen, Institute of Information Engineering, Chinese Academy of Sciences, School of Cyber Security, University of Chinese Academy of Sciences
Gang Shi, Institute of Information Engineering, Chinese Academy of Sciences, School of Cyber Security, University of Chinese Academy of Sciences
Kai Chen, Institute of Information Engineering, Chinese Academy of Sciences, School of Cyber Security, University of Chinese Academy of Sciences
Dan Meng, Institute of Information Engineering, Chinese Academy of Sciences, School of Cyber Security, University of Chinese Academy of Sciences

ECG-based Authentication using Timing-Aware Domain-Specific Architecture
Renato Cordeiro, San Jose State University
Dhruv Gajaria, University of Arizona
Ankur Limaye, University of Arizona
Tosiron Adegbija, University of Arizona
Nima Karimian, San Jose State University
Fatemeh Tebraniipoor, Santa Clara University

Efficient Return Address Verification Based on Dislocated Stack
Qizhen Xu, Chinese Academy of Sciences
Jinfeng Li, Chinese Academy of Sciences
Yongyue Li, Chinese Academy of Sciences
Liwei Chen, Chinese Academy of Sciences
Gang Shi, Chinese Academy of Sciences

Boosting Bit-Error Resilience of DNN Accelerators Through Median Feature Selection
Elbruz Ozen, University of California, San Diego
Alex Orailoglu, UC San Diego
Automated Controller and Sensor Configuration Synthesis using Dimensional Analysis
Marcus Pirron, Max Planck Institute for Software Systems
Damien Zufferey, Max Planck Institute for Software Systems (MPI-SWS)
Phillip Stanley-Marbell, University of Cambridge

Exploring Edge Computing for Multitier Industrial Control
YeHan Ma, Washington University in St. Louis
Chenyang Lu, Washington University in St. Louis
Bruno Sinopoli, Washington University in St. Louis
Shen Zeng, Washington University in St. Louis

Compositional Probabilistic Analysis of Temporal Properties over Stochastic Detectors
Ivan Ruchkin, University of Pennsylvania
Oleg Sokolsky, University of Pennsylvania
James Weimer, University of Pennsylvania
Tushar Hedao, University of Pennsylvania
Insup Lee, University of Pennsylvania

Fast Attack-Resilient Distributed State Estimator for Cyber-Physical Systems
Feng Yu, University of Central Florida
Raj Gautam Dutta, University of Central Florida
Teng Zhang, University of Central Florida
Yaodan Hu, University of Florida
Yier Jin, University of Florida

Quantitative Timing Analysis for Cyber-Physical Systems Using Uncertainty-Aware Scenario-Based Specifications
Ming Hu, East China Normal University
Wenxue Duan, Michigan Technological University
Min Zhang, East China Normal University
Tongquan Wei, East China Normal University
Mingsong Chen, East China Normal University
Dynamic Memory Bandwidth Allocation for Real-Time GPU-Based SoC Platforms
Homa Aghilanasab, University of Waterloo
Waqar Ali, University of Kansas at Lawrence
Heechul Yun, University of Kansas
Rodolfo Pellizzoni, University of Waterloo

HRM: Merging Hardware Event Monitors for Improved Timing Analysis of Complex MPSoCs
Sergi Vilardell, Polytechnic University of Catalonia
Roberto Santalla, Barcelona Supercomputing Center
Isabel Serra, Centre de Recerca Matematica
Enrico Mezzetti, Barcelona Supercomputing Center, BSC
Jaume Abella, Barcelona Supercomputing Center, BSC-CNS
Francisco J Cazorla, Barcelona Supercomputing Center

HopliteR*: Real-Time NoC for FPGA
Yilian Ribot, Cister Research Centre
Geoffrey Nelissen, Eindhoven University of Technology

EM-Fuzz: Augmented Firmware Fuzzing via Memory Checking
Jian Gao, School of Software, Tsinghua University
Yiwen Xu, School of Software, Tsinghua University
Yu Jiang, Tsinghua University
Zhe Liu, College of Computer Science and Technology, Nanjing University of Aeronautics and Astronautics
Wandi Chang, University of York
Xun Jiao, Department of Electrical and Computer Engineering, Villanova University
Jiaguang Sun, School of Software, Tsinghua University

eWASM: Practical Software Fault Isolation for Reliable Embedded Devices
Gregor Peach, George Washington University
Runyu Pan, George Washington University
Zhaoxi Wu, George Washington University
Gabriel Parmer, The George Washington University
Christopher Haster, ARM Ltd
Lucy Cherkasova, ARM Ltd
INDRA: Intrusion Detection using Recurrent Autoencoders in Automotive Embedded Systems  
Vipin Kumar Kukkala, Colorado State University  
Sooryaa Vignesh Thiruloga, Colorado State University  
Sudeep Pasricha, Colorado State University

SaeCAS: Secure Authenticated Execution using CAM-based Vector Storage  
Orlando Arias, University of Florida  
Dean Sullivan, University of Florida  
Haoqi Shan, University of Florida  
Yier Jin, University of Florida

Exposing Hardware Trojans in Embedded Platforms via Short-Term Aging  
Virinchi Roy Sarabha, New York University  
Prashanthi Krishnamurthy, NYU Tandon School of Engineering  
Hussam Amrouch, Karlsruhe Institute of Technology  
Joerg Hesskell, KIT  
Ramesh Karri, NYU  
Farshad Khorrami, NYU

Extending the Lifetime of MEDA Biochips by Selective Sensing on Microelectrodes  
Tung-Che Liang, Duke University  
Zhanwei Zhong, Duke University  
Miroslav Pajic, Duke University  
Krishnendu Chakrabarty, Duke University

Sparsity Turns Adversarial: Energy and Latency Attacks on Deep Neural Networks  
Sarada Krithivasan, Purdue University  
Sanchari Sen, Purdue University  
Anand Raghunathan, Purdue University
### Modular Design and Optimization of Biomedical Applications for Ultralow Power Heterogeneous Platforms
Elisabetta De Giovanni, École polytechnique fédérale de Lausanne
Fabio Montagna, Università di Bologna
Benoît Denkinger, École polytechnique fédérale de Lausanne
Simone Machetti, École polytechnique fédérale de Lausanne
Miguel Peón Quirós, EPFL ESL
Simone Benatti, Università di Bologna
Davide Rossi, University Of Bologna
Luca Benini, Università di Bologna and ETH Zurich
David Attenea, École Polytechnique Fédérale de Lausanne, EPFL

### Energy-Efficient Image Recognition System for Marine Life
Huseyin Seckin Demir, Arizona State University
Jennifer Blain Christen, Arizona State University
Sule Ozev, ASU

### Optimizing Sensor Deployment and Maintenance Costs for Large-Scale Environmental Monitoring
Xiaofan Yu, University of California, San Diego
Kazim Ergun, University Of California San Diego
Ludmila Cherkasova, Arm Research
Tajana Rosing, UCSD

### NEWER TRACK: ML-Based Accurate Tracking of In-Mouth Nutrient Sensors Position Using Spectrum-Wide Information
Amir Hosein Afandizadeh Zargari, University of California, Irvine
Manik Dautta, University of California, Irvine
Marzieh Ashrafi-Amiri, University of California, Irvine
Minjun Seo, University of California, Irvine
Peter Tseng, University of California, Irvine
Fadi Kurdahi, University of California, Irvine

### Hydrome: Reconfigurable Energy Storage for UAV Applications
Jiwon Kim, Yonsei University
Sungwoo Baek, Yonsei University
Yonghun Choi, Yonsei University
Junick Ahn, Yonsei University
Hojung Cha, Yonsei University
Enabling Latency-aware Data Initialization for Integrated CPU/GPU Heterogeneous Platform
Zhendong Wang, UT Dallas
Zihang Jiang, Tsinghua University
Zhen Wang, UT Dallas
Xulong Tang, University of Pittsburgh
Cong Liu, UT Dallas
Shouyi Yin, Tsinghua University
Yang Hu, UT Dallas

Error Diluting: Exploiting 3-D NAND Flash Process Variation for Efficient Read on LDPC-Based SSDs
Kong-Kiat Yong, National Chiao Tung University
Li-Pin Chang, National Chiao Tung University

On Minimizing Analog Variation Errors to Resolve the Scalability Issue of ReRAM-based Crossbar Accelerators
Yao-Wen Kang, National Taiwan University, CSIE
Chun-Feng Wu, National Taiwan University & Academia Sinica
Yuan-Hao Chang, Academia Sinica
Tei-Wei Kuo, Academia Sinica & National Taiwan University
Shu-Yin Ho, Macronix International Co., LTD

Fast DRAM PUFs on Commodity Devices
Jack Miskelly, Queen's University Belfast
Maire O'Neill, Queen's University Belfast

SEAL: User Experience-Aware Two-Level Swap for Mobile Devices
Changlong Li, City University of Hong Kong
Liang Shi, East China Normal University
Yu Liang, City University of Hong Kong
Chun Jason Xue, City University of Hong Kong
### Session 6A: CASES — Embedded Machine Learning: On Device Storage, Training, and Acceleration

**Date/Time**: September 23, 2020 (Wednesday) / 11:45 — 12:30 hrs  
**Moderator**: Jana Doppa, Washington State University, USA  
**Description**: Machine Learning (ML) algorithms play important roles in emerging embedded systems. This session presents papers highlighting ML algorithms fine-tuned for embedded systems.

<table>
<thead>
<tr>
<th>Title</th>
<th>Authors</th>
</tr>
</thead>
</table>
| Enabling On-Device CNN Training by Self-Supervised Instance Filtering and Error Map Pruning | Yawen Wu, University of Pittsburgh  
Zhepeng Wang, University of Pittsburgh  
Yiyu Shi, University of Notre Dame  
Jingtong Hu, University of Pittsburgh |
| DeepPrefetcher: A Deep Learning Framework for Data Prefetching in Flash Storage Devices | Gaddisa Olani Ganfure, Academia Sinica % National Tsing Hua University  
Chun-Feng Wu, National Taiwan University & Academia Sinica  
Yuan-Hao Chang, Academia Sinica  
Wei-Kuan Shih, National Tsing Hua University |
| WinDConv: A Fused Datapath CNN Accelerator for Power-efficient Edge Devices | Gopinath Vasanth Mahale, Samsung R&D Institute Bangalore  
Pramod Udappa, Samsung R&D Institute — Bangalore  
Kiran Kolar Chandrasekharan, Samsung R&D Institute — Bangalore  
Sehwan Lee, Samsung Advanced Institute of Technology, Suwon, Korea |
| UltraTrail: A Configurable Ultralow-Power TC-ResNet AI Accelerator for Efficient Keyword Spotting | Paul Palomero Bernardo, University of Tuebingen  
Christoph Gerum, University of Tuebingen  
Adrian Frischknecht, University of Tuebingen  
Konstantin Lubeck, University of Tuebingen  
Oliver Bringmann, University of Tuebingen / FZI |
<table>
<thead>
<tr>
<th>Session</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6B:CODES+ISSS — Memory and Scheduling</td>
<td>Memory accesses, memory architectures and scheduling play important roles in the performance of the embedded systems. This session explores the optimization for algorithms, memory architectures, virtual memory, thread migration and task scheduling.</td>
</tr>
</tbody>
</table>

### Shift-Limited Sort: Optimizing Sorting Performance on Skyrmion Memory-Based Systems

*Yun-Shan Hsieh*, National Tsing Hua University and National Taipei University of Technology  
*Po-Chun Huang*, Department of Electronic Engineering, National Taipei University of Technology  
*Ping-Xiang Chen*, National Tsing Hua University  
*Yuan-Hao Chang*, Academia Sinica  
*Kang Wang*, Fert Beijing Institute, BDRC, and Beihang University  
*Ming-Chang Yang*, The Chinese University of Hong Kong  
*Wei-Kuan Shih*, National Tsing Hua University

### ReSQM: Accelerating Database Operations Using ReRAM-based Content Addressable Memory

*Huize Li*, Huazhong University of Science and Technology  
*Hai Jin*, Huazhong University of Science and Technology  
*Long Zheng*, Huazhong University of Science and Technology  
*Xiaofei Liao*, Huazhong University of Science and Technology

### When Storage Response Time Catches Up with Overall Context Switch Overhead, What is Next?

*Chun-Feng Wu*, National Taiwan University & Academia Sinica  
*Yuan-Hao Chang*, Academia Sinica  
*Ming-Chang Yang*, The Chinese University of Hong Kong  
*Wei-Kuan Shih*, National Tsing Hua University  
*Tei-Wei Kuo*, Academia Sinica & National Taiwan University

### Hardware-Level Thread Migration to Reduce On-Chip Data Movement via Reinforcement Learning

*Quintin Fettes*, Ohio University  
*Avinash Karanth*, Ohio University  
*Razvan Bunescu*, Ohio University  
*Ahmed Louaj*, George Washington University  
*Kyle Shiflett*, Ohio University

### Runtime Task Scheduling using Imitation Learning for Heterogeneous Many-Core Systems

*Anish Krishnakumar*, Arizona State University  
*Samet Egemen Arda*, Arizona State University  
*A. Alper Goksoy*, Arizona State University  
*Sumit K. Mandal*, Arizona State University  
*Umit Ogras*, Arizona State University  
*Anderson Luiz Sartor*, Carnegie Mellon University  
*Radu Marculescu*, The University of Texas at Austin
Session 6C:EMSOFT — Modeling and Verification
Date/Time September 23, 2020 (Wednesday) / 11:45 — 12:30 hrs
Moderator Ichiro Hasuo, National Institute of Informatics, Japan
Description Formal methods for synthesis and verification of discrete and continuous systems.

Specification-Guided Automated Debugging of CPS Models
Nikhil Kumar Singh, IIT Kanpur
Indranil Saha, Indian Institute of Technology Kanpur

Mining Shape Expressions From Positive Examples
Ezio Bartocci, Vienna University of Technology
Jyotirmoy Deshmukh, University of Southern California
Felix Gigler, AIT Austrian Institute of Technology
Cristinel Mateis, AIT Austrian Institute of Technology
Dejan Nickovic, AIT Austrian Institute of Technology
Xin Qin, University of Southern California

Assume-Guarantee Distributed Synthesis
Rupak Majumdar, Kaushik Mallik, MPI-SWS
Anne-Kathrin Schmuck, Max Planck Institute for Software Systems (MPI-SWS)
Damien Zufferey, Max Planck Institute for Software Systems (MPI-SWS)

Online Signal Monitoring with Bounded Lag
Konstantinos Mamouras, Rice University
Zhifu Wang, Rice University

PAC Model Checking of Black-Box Continuous-Time Dynamical Systems
Bai Xue, Institute of Software Chinese Academy of Sciences
Miaomiao Zhang, School of Software Engineering, Tongji University, China
Arvind Easwaran, School of Computer Science and Engineering, Nanyang Technological University, Singapore
Qin Li, Software Engineering Institute, East China Normal University, China
Session 7A: CASES — Work-in-Progress

Work-in-Progress: Run-Time Accuracy Reconfigurable Stochastic Computing for Dynamic Reliability and Power Management
Shuyuan Yu, Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521
Han Zhou, Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521
Shaoyi Peng, Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521
Huussam Amrouch, Karlsruhe Institute of Technology, Chair for Embedded Systems (CES), Karlsruhe, Germany
Joerg Henkel, Karlsruhe Institute of Technology, Chair for Embedded Systems (CES), Karlsruhe, Germany
Sheldon X.-D. Tan, Department of Electrical and Computer Engineering, University of California, Riverside, CA 92521

Work-in-Progress: Smart Migration for Reliability Enhancement of 3D TLC NAND Flash Storage Systems
Yazhi Du, Soochow University Suzhou China
Jihua Gu, Soochow University Suzhou China
Zhongzhe Xiao, Soochow University Suzhou China
Min Huang, Soochow University Suzhou China

Work-in-Progress: A Lifelong Health Monitoring Framework in Processors
Xiao Hu, School of Computer National University of Defense Technology Changsha, P. R. of China, 410073
Yaohua Wang, School of Computer National University of Defense Technology Changsha, P. R. of China, 410073

Work-in-Progress: The Shift PUF: Technique for Squaring the Machine Learning Complexity of Arbiter-based PUFs
Yi Tang, New York University, NY
Donghang Wu, Peking University, China
Yongzhi Cao, Peking University, China
Marian Margraf, Freie Universität Berlin, Germany

Work-in-Progress: Towards Quality-Driven Approximate Software Generation for Accurate Hardware
Jorge Castro-Godínez, Chair for Embedded Systems (CES), Karlsruhe Institute of Technology (KIT), Germany, School of Electronics Engineering, Instituto Tecnológico de Costa Rica (TEC), Costa Rica
Muhammad Shafique, Institute of Computer Engineering, Vienna University of Technology (TU Wien), Austria, Division of Engineering, New York University Abu Dhabi, UAE
Jörg Henkel, Chair for Embedded Systems (CES), Karlsruhe Institute of Technology (KIT), Germany

Work-in-Progress: Page Reuse in Cyclic Thrashing of GPU Under Oversubscription
Dojin Park, Sungkyunkwan University Suwon, Republic of Korea
Hwansoo Han, Sungkyunkwan University Suwon, Republic of Korea

Work-in-Progress: Effective Profiling for Data-Intensive GPU Programs
Hwivwon Kim, College of ICE Sungkyunkwan University Suwon, Korea
Hyunjun Kim, College of ICE Sungkyunkwan University Suwon, Korea
Hwansoo Han, College of Computing Sungkyunkwan University Suwon, Korea
Session 7B: CODES+iSSS — Work-in-Progress

Work-in-Progress: Formal Verification of GCSE in the Scheduling of High-level Synthesis
Jian Hu, The Sixty-third Research Institute, National University of Defense Technology, NanJing, China
Yongyang Hu, The Sixty-third Research Institute, National University of Defense Technology, NanJing, China
Long Yu, The Sixty-third Research Institute, National University of Defense Technology, NanJing, China
Wentao Wang, College of Computer Science and Technology, National University of Defense Technology, ChangSha, China
Haitao Yang, The Sixty-third Research Institute, National University of Defense Technology, NanJing, China
Yun Kang, The Sixty-third Research Institute, National University of Defense Technology, NanJing, China
Jie Cheng, The Sixty-third Research Institute, National University of Defense Technology, NanJing, China

Work-in-Progress: A New Hardware Trojan Design: Distinguishing Between Trigger Inputs and Functional Inputs Is Difficult
Minghui Ge, dept. Electronic and Information Engineering (EIE) Nanjing University of Aeronautics and Astronautics (NUAA) Nanjing, China
Ying Zhang, dept. Electronic and Information Engineering (EIE) Nanjing University of Aeronautics and Astronautics (NUAA) Nanjing, China
Sen Li, dept. Electronic and Information Engineering (EIE) Nanjing University of Aeronautics and Astronautics (NUAA) Nanjing, China
Jiaqi Yao, dept. Electronic and Information Engineering (EIE) Nanjing University of Aeronautics and Astronautics (NUAA) Nanjing, China
Zhiming Mao, dept. Electronic and Information Engineering (EIE) Nanjing University of Aeronautics and Astronautics (NUAA) Nanjing, China
Xin Chen, dept. Electronic and Information Engineering (EIE) Nanjing University of Aeronautics and Astronautics (NUAA) Nanjing, China

Work-in-Progress: WiderFrame: An Automatic Customization Framework for Building CNN Accelerators on FPGAs
Lei Gong, School of Computer Science and Technology, University of Science and Technology of China
Chao Wang, School of Computer Science and Technology, University of Science and Technology of China
Xi Li, School of Computer Science and Technology, University of Science and Technology of China
Xuehai Zhou, School of Computer Science and Technology, University of Science and Technology of China

Shounak Chakraborty, Department of Computer Science, Norwegian University of Science and Technology (NTNU), Trondheim, Norway
Sangeet Saha, Embedded and Intelligent Systems Laboratory, University of Essex, Colchester, UK
Magnus Själander, Department of Computer Science, Norwegian University of Science and Technology (NTNU), Trondheim, Norway
Klaus McDonald-Maier, Embedded and Intelligent Systems Laboratory, University of Essex, Colchester, UK
Work-in-Progress: An Energy-aware Spiking Neural Network Hardware Mapping based on Particle Swarm Optimization and Genetic Algorithm
Junxiu Liu, School of Electronic Engineering, Guangxi Normal University, Guilin, China
Xingyue Huang, School of Electronic Engineering, Guangxi Normal University, Guilin, China
Dong Jiang, School of Electronic Engineering, Guangxi Normal University, Guilin, China
Yuling Luo, School of Electronic Engineering, Guangxi Normal University, Guilin, China

Work-in-Progress: GraphPage: RDF Graph in SSD Pages
Guohua Yan, College of Intelligence and Computing, Shenzhen Research Institute of Tianjin University, Tianjin University
Renhai Chen, College of Intelligence and Computing, Shenzhen Research Institute of Tianjin University, Tianjin University
Zhiyong Feng, College of Intelligence and Computing, Shenzhen Research Institute of Tianjin University, Tianjin University

Work-in-Progress: Accelerating Queries of MongoDB by an FPGA-based Storage Engine
Jinyu Zhan, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Junting Wu, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Wei Jiang, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Ying Li, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Jiaping Zhu, Tencent Technology Shenzhen Company Ltd, China

Work-in-Progress: Layering the monitoring action for improved flexibility and overhead control
Giacomo Valentino, Università degli Studi dell’Aquila
Tiziana Fanni, Università degli Studi di Sassari
Carlo Sau, Università degli Studi di Cagliari
Francesco Di Battista, Università degli Studi dell’Aquila

Work-in-Progress: Attention-Based Secure Feature Extraction in Near Sensor Processing
Pankaj Bhowmik, Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida
Jubael Hassan Pantho, Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida
Sujan Kumar Saha, Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida
Christophe Bobda, Department of Electrical and Computer Engineering, University of Florida, Gainesville, Florida

Work-in-Progress: Techniques for Design Analysis and Modification Based on ASAP Model
Ke Du, FEMTO-ST Institute, CNRS UMR 6174 Univ. Bourgogne Franche-Comté’s Belfort, France
Stéphane Domas, FEMTO-ST Institute, CNRS UMR 6174 Univ. Bourgogne Franche-Comté’s Belfort, France
Michel Leclercq, FEMTO-ST Institute, CNRS UMR 6174 Univ. Bourgogne Franche-Comté’s Belfort, France
Jing Liao, College of Computer Science and Software Engineering
Zhengda Li, College of Computer Science and Software Engineering
Yi Wang, College of Computer Science and Software Engineering, The National Engineering Laboratory for Big Data System Computing Technology, Shenzhen University, Shenzhen, China

Work-in-Progress: Model Stealing Defense with Hybrid Fuzzy Models
Zicheng Gong, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Wei Jiang, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Jinyu Zhan, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Ziwei Song, School of Information & Software Engineering, University of Electronic Science & Technology of China, China

Work-in-Progress: Heatmap-Aware Low-Cost Design to Resist Adversarial Attacks
Zhiyuan He, School of Information and Software Engineering, University of Electronic Science and Technology of China
Wei Jiang, School of Information and Software Engineering, University of Electronic Science and Technology of China
Jinyu Zhan, School of Information and Software Engineering, University of Electronic Science and Technology of China
Xupeng Wang, School of Information and Software Engineering, University of Electronic Science and Technology of China
Xiangyu Wen, School of Information and Software Engineering, University of Electronic Science and Technology of China

Alessio Colucci, Technische Universität Wien, Vienna, Austria
Alberto Marchisio, Technische Universität Wien, Vienna, Austria
Beatrice Bussolino, Politecnico di Torino, Turin, Italy
Maurizio Martina, Politecnico di Torino, Turin, Italy
Guido Masera, Politecnico di Torino, Turin, Italy
Vojtech Mrazek, Faculty of Information Technology, IT4Innovations Centre of Excellence, Brno University of Technology, Czech Republic
Muhammad Shafique, Technische Universität Wien, Vienna, Austria, Division of Engineering, New York University Abu Dhabi, UAE

Ryan Zelek, San Jose State University
Vignesh K. Venkateshwar, San Jose State University
Sai K. Duggineni, San Jose State University
Renu Dighe, San Jose State University
Hyeran Jeon, University of California, Merced

Giacomo Valente, DISIM/DEWS Università degli Studi dell’Aquila, Italy
Tania Di Mascio, DISIM/DEWS Università degli Studi dell’Aquila, Italy
Luigi Pomante, DISIM/DEWS Università degli Studi dell’Aquila, Italy
Vincenzo Stoico, DISIM/DEWS Università degli Studi dell’Aquila, Italy
Work-in-Progress: Application of Simulation-Based Methods on Autonomous Vehicle Control with Deep Neural Network

Yuji Date, Frontier Research Center Toyota Motor Corporation 1200 Mishuku, Susono, Shizuoka, Japan
Takeshi Baba, Frontier Research Center Toyota Motor Corporation 1200 Mishuku, Susono, Shizuoka, Japan
Bardh Hoxha, Toyota Research Institute-North America 1555 Woodridge Ave, Ann Arbor, Michigan, U.S
Tomoya Yamaguchi, Toyota Research Institute-North America 1555 Woodridge Ave, Ann Arbor, Michigan, U.S
Danil Prokhorov, Toyota Research Institute-North America 1555 Woodridge Ave, Ann Arbor, Michigan, U.S

Work-in-Progress: OpenMP Device Offloading for Embedded Heterogeneous Platforms

Lukas Sommer, Embedded Systems and Applications Group, TU Darmstadt, Germany
Andreas Koch, Embedded Systems and Applications Group, TU Darmstadt, Germany

Work-in-Progress: Integrated Performance Tuning of an IIoT Digital Twin

Padma Iyenghar, Software Engineering Research Group, University of Osnabrück, Germany
Sakhivel M. Sundaram, Delphi Technologies, Avenue de Luxembourg, 4940 Bascharage, Luxembourg
Elke Pulvermüller, Software Engineering Research Group, University of Osnabrück, Germany

Work-in-Progress: Progress-aware dynamic slack exploitation in mixed-critical systems

Angeliki Kritikakou, Univ Rennes, Inria, CNRS, IRISA, France
Stefanos Skalistis, Raytheon Technologies Research Center, Ireland

Work-in-Progress: Interpretability Derived Backdoor Attacks Detection in Deep Neural Networks

Xiangyu Wen, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Wei Jiang, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Jinyu Zhan, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Xupeng Wang, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Zhuyuan He, School of Information & Software Engineering, University of Electronic Science & Technology of China, China

Work-in-Progress: Synchronizing Real-Time Tasks in Time-Aware Networks

Eleftherios Kyriakakis, DTU Compute Technical University of Denmark Kgs. Lyngby, Denmark
Jens Sparsø, DTU Compute Technical University of Denmark Kgs. Lyngby, Denmark
Peter Puschner, Inst. of Computer Engineering TU Wien Vienna, Austria
Martin Schoeber, DTU Compute Technical University of Denmark Kgs. Lyngby, Denmark

Work-in-Progress: The rclc Executor: Domain-specific deterministic scheduling mechanisms for ROS applications on microcontrollers

Jan Staschulat, Corporate Research Robert Bosch GmbH Renningen, Germany
Ingo Lütkebohle, Corporate Research Robert Bosch GmbH Renningen, Germany
Ralph Lange, Corporate Research Robert Bosch GmbH Renningen, Germany
Work-in-Progress: An Insight into Fault Propagation in Deep Neural Networks
Ruoxu Sun, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Jinyu Zhan, School of Information & Software Engineering, University of Electronic Science & Technology of China, China
Wei Jiang, School of Information & Software Engineering, University of Electronic Science & Technology of China, China

Work-in-Progress: Multiform Logical Time & Space for Specification of Automated Driving Assistance Systems
Qian Liu, Shanghai Key Laboratory of Trustworthy Computing, East China Normal University, Shanghai 200062, China
Robert de Simone, INRIA Sophia Antipolis Méditerranée, Sophia Antipolis Cedex, France
Xiaohong Chen, Shanghai Key Laboratory of Trustworthy Computing, East China Normal University, Shanghai 200062, China
Jing Liu, Shanghai Key Laboratory of Trustworthy Computing, East China Normal University, Shanghai 200062, China

Work-in-Progress: A Game Theory Approach to Heterogeneous Resource Management
Lara Premi, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milano, Italy
Federico Reghenzani, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milano, Italy
Giuseppe Massari, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milano, Italy
William Fornaciari, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Milano, Italy

Work-in-Progress: Towards Highly Specialized, POSIX-compliant Software Stacks with Unikraft
Sharan Santhanam, NEC Laboratories Europe GmbH Heidelberg, Germany
Simon Kuenzer, NEC Laboratories Europe GmbH Heidelberg, Germany
Hugo Lefeuvre, NEC Laboratories Europe GmbH Heidelberg, Germany
Felipe Huici, NEC Laboratories Europe GmbH Heidelberg, Germany
Alexander Jung, Lancaster University NEC Laboratories Europe GmbH Heidelberg, Germany
Santiago Pagani, Robert Bosch GmbH NEC Laboratories Europe GmbH Heidelberg, Germany
George-Cristian Muraru, University Politehnica of Bucharest Bucharest, Romania
Stefano Stabelini, Xilinx, Inc San Jose, USA
Justin He, ARM Technology (China) Co., Ltd Shanghai, China
Jonathan Beri, Mountain View, USA

Work-in-Progress: Safety Analysis of Linear Discrete-time Stochastic Systems
Ratan Lal, Kansas State University
Pavithra Prabhakar, Kansas State University
Work-in-Progress: A Machine Learning based Approximate Computing Approach on Data Flow Graphs
Ye Wang, School of Computer Science and Technology Harbin Institute of Technology Harbin, China
Jian Dong, School of Computer Science and Technology Harbin Institute of Technology Harbin, China
Yanxin Liu, School of Computer Science and Technology Harbin Institute of Technology Harbin, China
Chunpei Wang, School of Computer Science and Technology Harbin Institute of Technology Harbin, China
Gang Qu, Department of Electrical and Computer Engineering and Institute of Systems Research University of Maryland College Park, USA

Work-in-Progress: Efficient Multi-Class Out-of-Distribution Reasoning for Perception Based Networks
Shreyas Ramakrishna, Vanderbilt University
Zahra Rahiminasab, Nanyang Technological University
Arvind Easwaran, Nanyang Technological University
Abhishek Dubey, Vanderbilt University