

Embedded Systems Week (ESWEEK) 2020

Program

Sun, Sep 20, 2020

9:00am

Tutorial 1: Creating Domain-Specific Modeling Languages - Hands on

🕒 9:00am - 1:00pm, Sep 20

Tutorials

A horrible lie exists in our industry today: it says that defining a graphical domain-specific languages (DSLs) is difficult and time-consuming. In this tutorial, we will lay bare this fallacy and demonstrate how simple and quick it is to create domain-specific languages and their generators. Using a hands-on approach you will define several modeling languages and generators within a few hours, learning principles and best practices proven in industrial experience.

The tutorial teaches practical, repeatable steps to invent and implement DSL. The language definition process reveals the characteristics of DSLs that enable generating working code from models:

- DSL is based on the concepts of problem domain rather than code
- Scope of the language narrowed down to a particular domain
- Language minimizes the effort needed to create, update and check the models

Experience on using at least one modeling tool is required. Experience on language creation is not required.

Participation: This tutorial is an interactive hands-on tutorial where participants will define several modeling languages. To keep the focus on language design rather than low-level implementation details, we will use a high-level language workbench. Participants who sign up in advance will receive a three-month license for MetaEdit+ Workbench, which they can install beforehand.

Embedded Systems Week uses Zoom for video conferencing, and we can use Zoom's breakout rooms for one-on-one help. Be prepared to use your microphone and show your screen for detailed questions on your language definition.

🗣️ Speakers

Juha-Pekka Tolvanen

Steven Kelly

Tutorial 2: Software-Defined Hardware - Digital Design with Chisel

🕒 9:00am - 1:00pm, Sep 20

Tutorials

To develop future more complex digital circuits in less time we need a better hardware description language than VHDL or Verilog. Chisel is a hardware construction language intended to speed up the development of digital hardware and hardware generators.


Chisel is a hardware construction language implemented as a domain-specific language in Scala. Therefore, the full power of a modern programming language is available to describe hardware and, more important, hardware generators. Chisel has been developed at UC Berkeley and successfully used for several tape outs of RISC-V by UC Berkeley students and a chip for a tensor processing unit by Google. Here at the Technical University of Denmark we use Chisel in the T-CREST project and in teaching digital electronics and advanced computer architecture.

In this tutorial we will give an overview of Chisel to describe circuits, how to use the Chisel tester functionality to test and simulate digital circuits, present how to synthesize circuits for an FPGA, and present advanced functionality of Chisel for the description of circuit generators.

The aim of the course is to get a basic understanding of a modern hardware description language and be able to describe simple circuits in Chisel. This course will give a basis to explore more advanced concepts of circuit generators written in Chisel/Scala. The intended audience is hardware designers with some

background in VHDL or Verilog, but Chisel is also a good first hardware language for software programmers entering into hardware design (e.g., porting software algorithms to FPGAs for speedup).

Participation: The Chisel tutorial is an interactive tutorial that also includes discussions between participants. Therefore, please make sure that your audio and video equipment works. Everyone participating needs to be online visible. Furthermore, for the hands-on lab you need to install some SW on your PC (Java 1.8 JDK and sbt). For details see: <https://github.com/schoeberl/chisel-lab/blob/master/Setup.md>

 **Speaker**
Martin Schoeberl

Tutorial 3: Out-of-Order Parallel Simulation of SystemC Models using the RISC Framework


🕒 9:00am - 1:00pm, Sep 20

Tutorials

The simulation of large SystemC models is slow due to the sequential nature of traditional simulators, such as the Accellera proof-of-concept reference implementation. Parallel Discrete Event Simulation (PDES) offers an order of magnitude speedup, but incurs obstacles due to the cooperative multi-threading semantics of IEEE SystemC.

This tutorial introduces and practices the Recoding Infrastructure for SystemC (RISC) framework which enables aggressive automatic parallelization of SystemC simulation by use of out-of-order PDES which can achieve two orders of magnitude speedup. RISC also features advanced thread-aware static analysis of SystemC models using a dedicated compiler and segment graph data structure that allow deep insight into the potential parallelization of design models at hand.

Participation: For hands-on participation, you will need a Linux account on a multi-core host with Docker access to download RISC (otherwise you are welcome to just watch the demos).

 **Speaker**
Rainer Doemer

5 Subsessions

- **Introduction to Out-of-Order Parallel Discrete Event Simulation**
🕒 9:00am - 9:40am, Sep 20
- **Overcoming the Obstacles of IEEE SystemC Semantics**
🕒 9:40am - 10:20am, Sep 20
- **RISC: Recoding Infrastructure for SystemC**
🕒 10:20am - 11:15am, Sep 20
- **Hands-on Practical Training with RISC Compiler and Simulator**
🕒 11:15am - 12:15pm, Sep 20
- **Hands-on Practical Analysis of Parallel Potential of SystemC Models**
🕒 12:15pm - 1:00pm, Sep 20

11:00am

Tutorial 4: Tasking Framework: An open-source software development library for on-board software systems

🕒 11:00am - 12:00pm, Sep 20

Tutorials

* This tutorial is a **live Q&A session** with **pre-recorded videos made available before the event**.

Tasking Framework is a C++ software development library and an event-driven multithreading execution platform. It is developed by the Institute for Software Technology, German Aerospace Center (DLR). Tasking Framework is dedicated to improve the reusability in developing embedded software systems and to reconcile the embedded software with model-driven software development. It can be used to develop, but not dedicated for, critical as well as non-critical embedded software on single-core as well as parallel architectures. Tasking Framework gives software developers the ability to implement their applications as task graphs with arbitrary activation patterns (periodic, aperiodic and sporadic) using a set of abstract classes with virtual methods. It is compatible with the POSIX-based operating systems, mainly Linux and RTEMS. The Tasking Framework was successfully used in, for instance, the attitude orbit control system of a satellite, the experiment control system on a sounding rocket, and in a lunar navigation system.

In this tutorial, we will present the main features of Tasking Framework, how to get it, use cases, and development process.

Participation: You can download Tasking Framework from here <https://github.com/DLR-SC/tasking-framework>. Pre-recorded videos are posted in seven parts in the different sub-sessions listed below.

Pre-recorded videos are also available [here](#).

Speakers

Zain Alabedin Haj Hammadeh

Olaf Maibaum

7 Subsessions

- **Introduction to the tutorial and agenda**
🕒 11:00am - 11:00am, Sep 20
- **Tasking Framework in a nutshell: motivation and basic features**
🕒 11:00am - 11:00am, Sep 20
- **Tasking Framework from A to Z**
🕒 11:00am - 11:00am, Sep 20
- **Tasking Framework in practice: Checkout + Compile**
🕒 11:00am - 11:00am, Sep 20
- **Tasking Framework in practice: Basic Functionalities**
🕒 11:00am - 11:00am, Sep 20
- **Tasking Framework in practice: Timing Functionalities**
🕒 11:00am - 11:00am, Sep 20
- **Outlook on development process and invitation to contribute**
🕒 11:00am - 11:00am, Sep 20

2:00pm

Work-in-Progress

🕒 2:00pm - 5:00pm, Sep 20

Work-in-Progress

There will be **NO live Q&A** for this session. **Asynchronous Q&A** via the Whova chat where authors will answer will be available throughout the whole week.

38 Subsessions

- **Work-in-Progress: Application of Simulation-Based Methods on Autonomous Vehicle Control with Deep Neural Network**
🕒 2:00pm - 5:00pm, Sep 20

- **Work-in-Progress: Integrated Performance Tuning of an IIoT Digital Twin**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Progress-aware dynamic slack exploitation in mixed-critical systems**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Interpretability Derived Backdoor Attacks Detection in Deep Neural Networks**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Synchronizing Real-Time Tasks in Time-Aware Networks**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: The rclc Executor: Domain-specific deterministic scheduling mechanisms for ROS applications on microcontrollers**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: An Insight into Fault Propagation in Deep Neural Networks**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Multiform Logical Time & Space for Specification of Automated Driving Assistance System**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: A Game Theory Approach to Heterogeneous Resource Management**
🕒 2:00pm - 5:00pm, Sep 20
- **Work in Progress: Distributed Decision-making for Safe and Secure Global Resource Management via Blockchain: Work-in-Progress**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Towards Highly Specialized, POSIX-compliant Software Stacks with Unikraft**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Safety Analysis of Linear Discrete-time Stochastic Systems**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: A Machine Learning based Approximate Computing Approach on Data Flow Graphs**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Efficient Multi-Class Out-of-Distribution Reasoning for Perception Based Networks**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: OpenMP Device Offloading for Embedded Heterogeneous Platforms**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Formal Verification of GCSE in the Scheduling of High-level Synthesis**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: A New Hardware Trojan Design: Distinguishing Between Trigger Inputs and Functional Inputs Is Difficult**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: WiderFrame: An Automatic Customization Framework for Building CNN Accelerators on FPGAs**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: RePAiR: A Strategy for Reducing Peak Temperature while**

Enhancing Accuracy of Approximate Real-Time Computing

🕒 2:00pm - 5:00pm, Sep 20

- **Work-in-Progress: An Energy-aware Spiking Neural Network Hardware Mapping based on Particle Swarm Optimization and Genetic Algorithm**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: GraphPage: RDF Graph in SSD Pages**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Accelerating Queries of MongoDB by an FPGA-based Storage Engine**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Layering the monitoring action for improved flexibility and overhead control**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Attention-Based Secure Feature Extraction in Near Sensor Processing**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Techniques for Design Analysis and Modification Based on ASAP Model**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Meta-Chain: User-Aware Cross-Layer Space Allocation Strategy for Blockchain Storage Systems**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Model Stealing Defense with Hybrid Fuzzy Models**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Heatmap-Aware Low-Cost Design to Resist Adversarial Attacks**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: A Fast Design Space Exploration Framework for the Deep Learning Accelerators**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Enabling Edge-based Self-Navigation in Earthquake-Struck Zones**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: An Electronic System-Level Methodology for HW/SW Co-Design of Monitorable Embedded Systems: the "Design for Monitorability" Project**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Run-Time Accuracy Reconfigurable Stochastic Computing for Dynamic Reliability and Power Management**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Smart Migration for Reliability Enhancement of 3D TLC NAND Flash Storage Systems**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: A Lifelong Health Monitoring Framework in Processors**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: The Shift PUF: Technique for Squaring the Machine Learning Complexity of Arbiter-based PUFs**
🕒 2:00pm - 5:00pm, Sep 20
- **Work-in-Progress: Towards Quality-Driven Approximate Software Generation for Accurate Hardware**
🕒 2:00pm - 5:00pm, Sep 20

- **Work-in-Progress: Page Reuse in Cyclic Thrashing of GPU Under Oversubscription**
🕒 2:00pm - 5:00pm, Sep 20
- **Effective Profiling for Data-Intensive GPU Programs: Work-in-Progress**
🕒 2:00pm - 5:00pm, Sep 20

Mon, Sep 21, 2020

9:30am

ESWEEK Opening

🕒 9:30am - 9:55am, Sep 21

Plenary

Opening remarks

🗣️ Speakers

Tulika Mitra

Andreas Gerstlauer

10:00am

Keynote: Skin-Like Wireless Wearables – From Premature Babies in the NICU to Patients with COVID-19

🕒 10:00am - 10:55am, Sep 21

Plenary

Speaker: [Professor John A. Rogers](#), *Northwestern University*

Recent global events are reshaping the geopolitical and socio-economic landscape in ways that will likely alter research priorities for at least a generation – a broad consensus is that long-term solutions to the underlying societal challenges will only occur through innovative technologies and advanced medicines, as life-saving diagnostics, digital biosensors, therapeutics and preventatives. This talk will outline work that intersects with essential unmet needs in this broader context, specifically in the form of skin-like wireless wearables for continuous monitoring of physiological status with clinical-grade precision. The focus is on foundational ideas in materials, design and manufacturing, with examples of devices designed for patient populations that range from premature babies in neonatal intensive care units to COVID-19 patients in the hospital and the home – both deployed locally within the medical complex here in Chicago and globally in clinics across lower and middle income countries in Africa and Central America.

🗣️ Speaker

John Rogers

11:00am

CASES Session 1A: Memory Technologies

🕒 11:00am - 11:40am, Sep 21

CASES

** indicates Best Paper Candidate*

Moderator: [Sudeep Pasricha](#), *Colorado State University, USA*

Memory has been a key component of various computing platforms starting from mobile devices to high-performance computing (HPC) systems. This session presents papers showcasing recent advances on memory technologies.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Hardware Memory Management for Future Mobile Hybrid Memory Systems**
🕒 11:00am - 11:40am, Sep 21
- * **Patch-Based Data Management for Dual-copy Buffers in RAID-Enabled SSDs**
🕒 11:00am - 11:40am, Sep 21
- **Polyhedral Compilation for Racetrack Memories**
🕒 11:00am - 11:40am, Sep 21
- **AxFTL: Exploiting Error Tolerance for Extending Lifetime of NAND Flash Storage**
🕒 11:00am - 11:40am, Sep 21
- **Optimization of Intercache Traffic Entanglement in Tagless Caches with Tiling Opportunities**
🕒 11:00am - 11:40am, Sep 21

CODES+ISSS Session 1B: Neural Network Acceleration

🕒 11:00am - 11:40am, Sep 21

CODES+ISSS

* *indicates Best Paper Candidate*

Moderator: Yuan-Hao Chang, Academia Sinica, Taiwan

Deep learning and neural networks are increasingly becoming a key component of embedded systems across numerous application domains. This session explores both the design of energy-efficient and high-performance neural network accelerators and design space exploration methods to assist in designing those accelerators.

Pre-recorded videos are also available [here](#).

5 Subsessions

- * **Everything Leaves Footprints: Hardware Accelerated Intermittent Deep Inference**
🕒 11:00am - 11:40am, Sep 21
- **FSA: A Fine-Grained Systolic Accelerator for Sparse CNNs**
🕒 11:00am - 11:40am, Sep 21
- * **StereoEngine: An FPGA-based Accelerator for Real-Time High-quality Stereo Estimation with Binary Neural Network**
🕒 11:00am - 11:40am, Sep 21
- **SuperSlash: A Unified Design Space Exploration and Model Compression Methodology for Design of Deep Learning Accelerators With Reduced Off-Chip Memory Access Volume**
🕒 11:00am - 11:40am, Sep 21
- **WinoNN: Optimizing FPGA-based Convolutional Neural Network Accelerators Using Sparse Winograd Algorithm**
🕒 11:00am - 11:40am, Sep 21

EMSOFT Session 1C: Real-Time Scheduling

🕒 11:00am - 11:40am, Sep 21

EMSOFT

* *indicates Best Paper Candidate*

Moderator: Tarek Abdelzaher, University of Illinois at Urbana Champaign, USA

Scheduling algorithms and analyses with a focus on real-time and energy. Namely, (a) a novel schedulability analyses of suspension-aware EDF on uniprocessor systems for both sporadic and periodic task sets; (b) static scheduling using Integer Linear Programming of task graphs for actor networks onto multi-core ARM big.LITTLE CPUs with discrete voltage and frequency scaling; (c) new techniques to improve the computation of the demand-bound function for analyzing the feasibility and schedulability of real-time tasks; (d) a quantitative-verification framework for precedence-aware competitive analysis with a GPU-based analysis of well-known schedulers from the literature; and (e) new algorithms for real-time dynamic task scheduling based on directed acyclic graphs taking into account energy and reliability.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Suspension-Aware Earliest-Deadline-First Scheduling Analysis**
🕒 11:00am - 11:40am, Sep 21
- **Static Scheduling of Moldable Streaming Tasks with Task Fusion for Parallel Systems with DVFS**
🕒 11:00am - 11:40am, Sep 21
- *** Efficient Feasibility Analysis for Graph-based Real-Time Task Systems**
🕒 11:00am - 11:40am, Sep 21
- **Precedence-aware Automated Competitive Analysis of Real-time Scheduling**
🕒 11:00am - 11:40am, Sep 21
- **Dynamic DAG Scheduling on Multiprocessor Systems: Reliability, Energy and Makespan**
🕒 11:00am - 11:40am, Sep 21

11:45am

CASES Session 2A: Energy-efficient ML for IoT and Edge Devices

🕒 11:45am - 12:25pm, Sep 21

CASES

** indicates Best Paper Candidate*

Moderator: Ryan Kim, Colorado State University, USA

Advances in Machine Learning (ML) algorithms are key for the successful deployment of IoT and edge devices. This session focuses on application of ML algorithms in resource constraint environments.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Fusion-Catalyzed Pruning for Optimizing Deep Learning on Intelligent Edge Devices**
🕒 11:45am - 12:25pm, Sep 21
- *** Efficient Scheduling of Irregular Network Structures on CNN Accelerators**
🕒 11:45am - 12:25pm, Sep 21
- **FSpiNN: An Optimization Framework for Memory-Efficient and Energy-Efficient Spiking Neural Networks**
🕒 11:45am - 12:25pm, Sep 21
- **Analyzing Deep Learning for Time-Series Data through Adversarial Lens in Mobile and IoT Applications**
🕒 11:45am - 12:25pm, Sep 21
- **MacLeR: Machine Learning-Based Runtime Hardware Trojan Detection in Resource-Constrained IoT Edge Devices**
🕒 11:45am - 12:25pm, Sep 21

CODES+ISSS Session 2B: Multicore and Approximate Architectures

🕒 11:45am - 12:25pm, Sep 21

CODES+ISSS

Moderator: Liang Shi, East China Normal University, China

High-performance and energy-efficient multicore architectures are widely utilized within modern embedded systems. This session presents novel methods for approximate computing, approximate communication, time-predictable memory architectures, and more accurate power estimation methods.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Learning-based Quality Management for Approximate Communication in Networks-on-Chip**
🕒 11:45am - 12:25pm, Sep 21
- **Aggressive Fine-Grained Power Gating of NoC Buffers**
🕒 11:45am - 12:25pm, Sep 21
- **Meshed Bluetree: Time-Predictable Multi-Memory Interconnect for Multi-Core Architectures**
🕒 11:45am - 12:25pm, Sep 21
- **Risk-5: Controlled approximations for RISC-V**
🕒 11:45am - 12:25pm, Sep 21
- **A Lightweight Nonlinear Methodology to Accurately Model Multi-Core Processor Power**
🕒 11:45am - 12:25pm, Sep 21

EMSOFT Session 2C: Energy-Aware Applications and Techniques

🕒 11:45am - 12:25pm, Sep 21

EMSOFT

Moderator: Lothar Thiele, ETH Zürich, Switzerland

Techniques and applications with a focus on optimizing battery performance and energy use. Namely, (a) a system for reducing the state saved for tasks in an intermittent computing system; (b) an approach for planning battery-powered payload utilization in small, low-earth orbit satellites; (c) the optimization of discharge efficiency for multi-cell batteries using safety-supplemented hardware and machine learning, evaluated on a hardware prototype; (d) a scheme for maximizing drone flight time while safely using its battery based on state-of-charge information; and (e) a probabilistic energy prediction strategy with precise mixed-criticality scheduling that uses dynamic voltage and frequency scaling to minimize energy use while still guaranteeing timing correctness.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **LATICS: A Low-overhead Adaptive Task-based Intermittent Computing System**
🕒 11:45am - 12:25pm, Sep 21
- **Managing Fleets of LEO Satellites: Non-Linear, Optimal, Efficient, Scalable, Usable, and Robust**
🕒 11:45am - 12:25pm, Sep 21
- **Optimizing Discharging Efficiency of Reconfigurable Battery with Deep**

Reinforcement Learning

🕒 11:45am - 12:25pm, Sep 21

- **Optrone: Maximizing Performance and Energy Resources of Drone Batteries**
🕒 11:45am - 12:25pm, Sep 21
- **Optimizing Energy in Non-preemptive Mixed-Criticality Scheduling by Exploiting Probabilistic Information**
🕒 11:45am - 12:25pm, Sep 21

12:30pm

Meet the ESWEEK organizers and sponsoring society representatives

🕒 12:30pm - 1:00pm, Sep 21

Plenary

Meet the organizers of ESWEEK.

CASES Networking

🕒 12:30pm - 1:00pm, Sep 21

CASES

CODES+ISSS Networking

🕒 12:30pm - 1:00pm, Sep 21

CODES+ISSS

EMSOFT Networking

🕒 12:30pm - 1:00pm, Sep 21

EMSOFT

Tue, Sep 22, 2020

7:30am

European Industrial Session

🕒 7:30am - 9:00am, Sep 22

Industry Session

Moderator: Rainer Leupers, RWTH Aachen University, Germany

This session showcases eight European technology transfer experiments funded by the Horizon 2020 innovation action TETRAMAX ("Technology Transfer via Multinational Application Experiments"). The experiments are the result of collaboration between academic researchers and small or medium enterprises in different EU countries. Presentations will cover novel applications and products involving sensors, IoT applications, drones, embedded controllers, FPGAs in the cloud, and GPU applications.

9 Subsessions

- **TETRAMAX: Innovation hub for digitizing European SMEs**
🕒 7:30am - 7:40am, Sep 22
- **Low-power IoT turn-key solution for Smart Agriculture: from field sensors to DSS service platform**
🕒 7:40am - 7:50am, Sep 22
- **BLEper: A low-cost outdoor location tracking solution for shoreline safety**
🕒 7:50am - 8:00am, Sep 22

- **A smart capsule for the delivery and monitoring of blood and hemocomponents**
⌚ 8:00am - 8:10am, Sep 22
- **Embedded system as central element an intelligent industrial mobile tanking solution**
⌚ 8:10am - 8:20am, Sep 22
- **Open FPGA data Science Platform: Accelerating ML instantly by utilizing FPGAs**
⌚ 8:20am - 8:30am, Sep 22
- **ROSSPAD, bringing radiation detection capability to IoT**
⌚ 8:30am - 8:40am, Sep 22
- **TETRAMAX-ANDREAS: Scheduling solutions for AI training jobs in on demand GPU Systems**
⌚ 8:40am - 8:50am, Sep 22
- **A Low Complexity Bluetooth Direction-Finding apparatus, a comparison**
⌚ 8:50am - 9:00am, Sep 22

9:00am

Industrial Session Networking

⌚ 9:00am - 9:25am, Sep 22

Industry Session

9:30am

Test of Time Awards

⌚ 9:30am - 9:55am, Sep 22

Plenary

Presentation of the Test-of-Time Awards

10:00am

Keynote: Digital Twins: Challenges and Opportunities in Various Industries

⌚ 10:00am - 10:55am, Sep 22

Plenary

Speaker: Dr. Prith Banerjee, CTO, ANSYS

Various industries such as Manufacturing, Energy and Utilities, Automotive, Aerospace and Defense, Logistics and Transportation, and Building Management, have proposed the use of Digital Twins to aid the Design, Analysis, Build, Manufacturing and Operations phases of asset-intensive industries. Digital Twins have a physical asset, a virtual asset (a simulation model of the asset), and a two-way information flow between the physical and virtual worlds using an IOT platform. While most companies use data-based analytics and machine learning to build Digital Twins, they require lots of training data and the accuracy is limited to the observed data. Some industries have started using physics based simulation to build digital twins and while these approaches are accurate they require long computation times to deploy. Most recently, companies are using Hybrid approaches combining data-based analytics and physics-based approaches to build these digital twins that are very accurate and require less training data, and drive high operational efficiency of assets and process industries and manufacturing plants. In this talk we will discuss the challenges and opportunities of digital twins in various industries and the latest research approaches.

🗣️ **Speaker**
Prith Banerjee

11:00am

CASES Session 3A: Processor Architecture

🕒 11:00am - 11:40am, Sep 22

CASES

** indicates Best Paper Candidate*

Moderator: Ganapati Bhat, Washington State University, USA

Heterogeneous processors have been at the heart of the state-of-the-art many-core architectures. This session pre-sents latest scheduling, run-time management, and optimization of processor architecture under emerging work-loads.

Pre-recorded videos are also available [here](#).

5 Subsessions

- *** Fast and Correct Load-Link/Store-Conditional Instruction Handling in DBT Systems**
🕒 11:00am - 11:40am, Sep 22
- **VisSched: An Auction based Scheduler for Vision Workloads on Heterogeneous Processors**
🕒 11:00am - 11:40am, Sep 22
- **Dynamic Power and Energy Management for NCFET-based Processors**
🕒 11:00am - 11:40am, Sep 22
- **FINDER: Find Efficient Parallel Instructions for ASIPs to Improve Performance of Large Applications**
🕒 11:00am - 11:40am, Sep 22
- **NPU Thermal Management**
🕒 11:00am - 11:40am, Sep 22

CODES Session 3B: HLS and System Design

🕒 11:00am - 11:40am, Sep 22

CODES+ISSS

** indicates Best Paper Candidate*

Moderator: Ann Gordon-Ross, University of Florida, USA

The increasing complexity of embedded systems demands efficient system design methodologies to assist designers in optimizing and secure these systems. This session presents high-level synthesis and system-level design methods that can optimize design for different underlying architectures.

Pre-recorded videos are also available [here](#).

4 Subsessions

- *** Tensor Optimization for High-level Synthesis Design Flows**
🕒 11:00am - 11:40am, Sep 22
- **AnyHLS: High-Level Synthesis with Partial Evaluation**
🕒 11:00am - 11:40am, Sep 22
- **Standing on the Shoulders of Giants: Hardware and Neural Architecture Co-Search with Hot Start**
🕒 11:00am - 11:40am, Sep 22
- **MeXT-SE: A Design Tool to Transparently Generate Secure MPSoC**
🕒 11:00am - 11:40am, Sep 22

EMSOFT Session 3C: Hybrid Systems and Neural Networks

🕒 11:00am - 11:40am, Sep 22

EMSOFT

** indicates Best Paper Candidate*

Moderator: Sylvie Putot, *École polytechnique, France*

Falsification, verification, and applications of hybrid systems models and neural networks. The talks cover (a) a method for reducing stochastic reachability to adversary reachability of random ordinary differential equations over both finite and infinite time horizons; (b) an enhancement to the continuous and discrete post operators used to analyze reachability in linear hybrid systems, ensuring that most computations occur in a low-dimensional state space; (c) a falsification technique for hybrid systems based on searching an unconstrained space guided by the robustness of points in a corresponding space with input constraints; (d) an analysis of neural network output ranges based on iterative convex polygonal over-approximations encoded as a mixed-integer linear programming problem; and (e) a pruned reinforcement learning-based approach to optimize the frequency of background cleaning of log-structured file systems.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Safety Verification for Random Ordinary Differential Equations**

🕒 11:00am - 11:40am, Sep 22

- *** Reachability Analysis of Linear Hybrid Systems via Block Decomposition**

🕒 11:00am - 11:40am, Sep 22

- **Hybrid System Falsification under (In)equality Constraints via Search Space Transformation**

🕒 11:00am - 11:40am, Sep 22

- **Divide and Slide: Layer-Wise Refinement for Output Range Analysis of Deep Neural Networks**

🕒 11:00am - 11:40am, Sep 22

- **Pruning Deep Reinforcement Learning for Dual User Experience and Storage Lifetime Improvement on Mobile Devices**

🕒 11:00am - 11:40am, Sep 22

11:45am

CASES Session 4A: Design Space Exploration

🕒 11:45am - 12:25pm, Sep 22

CASES

Moderator: Muhammad Shafique, *Vienna University of Technology, Austria*

Resource management is essential to improve performance and energy-efficiency of processors. This session pre-sents papers addressing high level synthesis, memory management and security challenges in processor architectures.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Toward Speculative Loop Pipelining for High-Level Synthesis**

🕒 11:45am - 12:25pm, Sep 22

- **Leveraging Prior Knowledge for Effective Design-Space Exploration in High-Level Synthesis**

🕒 11:45am - 12:25pm, Sep 22

- **Maskara: Compilation of a Masking Countermeasure with Optimised Polynomial Interpolation**
🕒 11:45am - 12:25pm, Sep 22
- **Boosting User Experience via Foreground-Aware Cache Management in UFS Mobile Devices**
🕒 11:45am - 12:25pm, Sep 22
- **Combating Enhanced Thermal Covert Channel in Multi-/Many-core Systems with Channel-aware Jamming**
🕒 11:45am - 12:25pm, Sep 22

CODES+ISSS Session 4B: Security and Authentication

🕒 11:45am - 12:25pm, Sep 22

CODES+ISSS

Moderator: Brett Meyer, McGill University, Canada

Safety-critical and life-critical systems require both security and resilience. This sessions presents new methods for control-flow integrity, authentication, and bit error resilience.

Pre-recorded videos are also available [here](#).

4 Subsessions

- **ABCFl: Fast and Lightweight Fine-grained Hardware-assisted Control Flow Integrity**
🕒 11:45am - 12:25pm, Sep 22
- **ECG-based Authentication using Timing-Aware Domain-Specific Architecture**
🕒 11:45am - 12:25pm, Sep 22
- **Efficient Return Address Verification Based on Dislocated Stack**
🕒 11:45am - 12:25pm, Sep 22
- **Boosting Bit-Error Resilience of DNN Accelerators Through Median Feature Selection**
🕒 11:45am - 12:25pm, Sep 22

EMSOFT Session 4C: Control, Sensing, and Probability

🕒 11:45am - 12:25pm, Sep 22

EMSOFT

Moderator: Guillaume Baudart, IBM Watson, USA

Implementing and analyzing Cyber-Physical Systems with a particular focus on handling uncertainty and sensors. The talks present (a) a design methodology for co-designing software controllers and sensing capabilities that exploits physical units in the model to estimate unobservable state components; (b) a scheme for optimizing industrial control performance by switching between local controllers and edge servers in response to changing wireless network conditions; (c) a framework for modeling and analyzing noisy run-time monitoring systems using temporal logic and probabilistic techniques with an evaluation on an autonomous underwater vehicle; (d) a distributed algorithm that produces bounded state estimation errors in the presence of attacks and compromised sensors demonstrated using false data injection into a platoon of vehicles; and (e) an extension of UML sequence diagrams for modeling stochastic system inputs, message processing time, and network delays, with support for statistical model checking.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Automated Controller and Sensor Configuration Synthesis using Dimensional Analysis**

🕒 11:45am - 12:25pm, Sep 22

- **Exploring Edge Computing for Multi-Tier Industrial Control**

🕒 11:45am - 12:25pm, Sep 22

- **Compositional Probabilistic Analysis of Temporal Properties over Stochastic Detectors**

🕒 11:45am - 12:25pm, Sep 22

- **Fast Attack-Resilient Distributed State Estimator for Cyber-Physical Systems**

🕒 11:45am - 12:25pm, Sep 22

- **Quantitative Timing Analysis for Cyber-Physical Systems using Uncertainty-Aware Scenario-Based Specifications**

🕒 11:45am - 12:25pm, Sep 22

EMSOFT Session 4D: Systems-level Hardware and Software

🕒 11:45am - 12:25pm, Sep 22

EMSOFT

** indicates Best Paper Candidate*

Moderator: Bryan Ward, MIT Lincoln Laboratory, USA

Techniques for GPUs, MPSoCs, FPGAs, NoCs, Firmware, and microcontrollers. Namely, (a) a memory bandwidth allocation scheme for SoC platforms that dynamically monitors real-time applications and increases the bandwidth for best-effort applications when safe to do so; (b) an approach for reading and merging hardware event monitors across different runs for measurement-based time budgeting and verification, applied to an NXP T2080 platform; (c) increased support for real-time systems on HopliteRT, an FPGA-based network-on-chip, including the addition of priority-based routing and a new timing analysis; (d) a firmware vulnerability detection technique that tightly integrates fuzzing with real-time memory checking and which found sixteen previously unknown vulnerabilities; and (e) an adaptation of an existing application sandbox to resource-constrained microcontrollers aimed at practical use on IoT devices.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Dynamic Memory Bandwidth Allocation for Real-Time GPU-Based SoC Platforms**

🕒 11:45am - 12:25pm, Sep 22

- **HRM: Merging Hardware Event Monitors for Improved Timing Analysis of Complex MPSoCs**

🕒 11:45am - 12:25pm, Sep 22

- **HopliteRT*: Real-Time NoC for FPGA**

🕒 11:45am - 12:25pm, Sep 22

- *** EM-Fuzz: Augmented Firmware Fuzzing via Memory Checking**

🕒 11:45am - 12:25pm, Sep 22

- **eWASM: Practical Software Fault Isolation for Reliable Embedded Devices**

🕒 11:45am - 12:25pm, Sep 22

12:30pm

Meet the Test of Time Award winners

🕒 12:30pm - 1:00pm, Sep 22

Plenary

CASES Networking

🕒 12:30pm - 1:00pm, Sep 22

CASES

CODES+ISSS Networking

🕒 12:30pm - 1:00pm, Sep 22

CODES+ISSS

EMSOFT Networking

🕒 12:30pm - 1:00pm, Sep 22

EMSOFT

1:00pm

Industry Live Q&A Session - Xilinx embedded solutions

🕒 1:00pm - 1:30pm, Sep 22

Industry Session

Cathal McCabe, *Xilinx University Program*, will give a 15 – 20 minutes introduction on the embedded solutions portfolio followed by the opportunity to ask questions.

🗣️ Speakers

Hugo Andrade

Cathal McCabe

1:30pm

Embedded Systems Educational Resources from ARM

🕒 1:30pm - 2:00pm, Sep 22

Industry Session

Richard Buttrey and Robert Iannello from Arm Education will provide an overview of the digital resources created for academics and students to assist in the transition to online learning in the wake of the COVID-19 pandemic.

🗣️ Speakers

Robert Iannello

Richard Buttrey

Wed, Sep 23, 2020

9:30am

Best Paper and Other Awards

🕒 9:30am - 9:55am, Sep 23

Plenary

Presentation of Best Paper Awards for CASES, CODES+ISSS, EMSOFT, ACM Transactions on Embedded Computing Systems (TECS), and SIGBED Frank Anger Memorial Award.

10:00am

Panel - Post COVID-19 Cyber Security – The Challenges and Solutions

🕒 10:00am - 10:55am, Sep 23

Plenary

Moderator: Sri Parameswaran – UNSW

Panelists: Richard Buckland – UNSW, Farinaz Koushanfar – UCSD, Nasir Memon – NYU, Ingrid Verbauwhede – KU Leuven

Speaker

Sri Parameswaran

11:00am

CASES Session 5A: Security and Reliability

🕒 11:00am - 11:40am, Sep 23

CASES

Moderator: Sai Manoj, *George Mason University, USA*

Secure and Reliable system design is essential for building a sustainable computing eco system. This session high-lights papers addressing security and reliability challenges at various levels of computing stack starting from auto-motive to embedded systems to biochips.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **INDRA: Intrusion Detection using Recurrent Autoencoders in Automotive Embedded Systems**
🕒 11:00am - 11:40am, Sep 23
- **SAECAS: Secure Authenticated Execution using CAM-based Vector Storage**
🕒 11:00am - 11:40am, Sep 23
- **Exposing Hardware Trojans in Embedded Platforms via Short-Term Aging**
🕒 11:00am - 11:40am, Sep 23
- **Extending the Lifetime of MEDA Biochips by Selective Sensing on Microelectrodes**
🕒 11:00am - 11:40am, Sep 23
- **Sparsity Turns Adversarial: Energy and Latency Attacks on Deep Neural Networks**
🕒 11:00am - 11:40am, Sep 23

CODES+ISSS Session 5B: Biomedical, Environmental, and UAV Systems

🕒 11:00am - 11:40am, Sep 23

CODES+ISSS

Moderator: Gunar Schirner, *Northeastern University, USA*

This session explores the design and optimization to embedded system for remote health monitoring, underwater marine life imaging, and large-scale environmental monitoring.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Modular Design and Optimization of Biomedical Applications for Ultra-Low Power Heterogeneous Platforms**
🕒 11:00am - 11:40am, Sep 23
- **Energy-Efficient Image Recognition System for Marine Life**

🕒 11:00am - 11:40am, Sep 23

- **Optimizing Sensor Deployment and Maintenance Costs for Large-Scale Environmental Monitoring**

🕒 11:00am - 11:40am, Sep 23

- **NEWERTRACK: ML-Based Accurate Tracking of In-Mouth Nutrient Sensors Position Using Spectrum-Wide Information**

🕒 11:00am - 11:40am, Sep 23

- **Hydrone: Reconfigurable Energy Storage for UAV Applications**

🕒 11:00am - 11:40am, Sep 23

EMSOFT Session 5C: Memory and GPUs

🕒 11:00am - 11:40am, Sep 23

EMSOFT

Moderator: Nan Guan, *The Hong Kong Polytechnic University*

Improving the performance and exploiting the properties of GPUs, SSDs, ReRAMs, DRAMs, and paging on portable devices. The talks present (a) a framework for latency-aware data initialization of GPUs, such as the NVIDIA TX2 and AGX platforms, to better support mobile/edge applications; (b) a technique that exploits bit-error rate variation among vertical layers of 3D NAND flash to improve read throughput and latency in multichip SSDs; (c) an adaptive data-manipulation strategy for reducing analog variation errors in ReRAM-based crossbar accelerators for neural network applications; (d) a set of software-based algorithms for deriving physical unclonable functions from DRAM by altering timing parameters; and (e) a framework for swapping on mobile devices that maximizes application caching capability while minimizing negative impacts on users.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Enabling Latency-aware Data Initialization for Integrated CPU/GPU Heterogeneous Platform**

🕒 11:00am - 11:40am, Sep 23

- **Error Diluting: Exploiting 3D-NAND Flash Process Variation for Efficient Read on LDPC-based SSDs**

🕒 11:00am - 11:40am, Sep 23

- **On Minimizing Analog Variation Errors to Resolve the Scalability Issue of ReRAM-based Crossbar Accelerators**

🕒 11:00am - 11:40am, Sep 23

- **Fast DRAM PUFs on Commodity Devices**

🕒 11:00am - 11:40am, Sep 23

- **SEAL: User Experience Aware Two-Level Swap for Mobile Devices**

🕒 11:00am - 11:40am, Sep 23

11:45am

CASES Session 6A: Embedded Machine Learning: On Device Storage, Training, and Acceleration

🕒 11:45am - 12:25pm, Sep 23

CASES

Moderator: Jana Doppa, *Washington State University, USA*

Machine Learning (ML) algorithms play important roles in emerging embedded systems. This session presents papers highlighting ML algorithms fine-tuned for embedded systems.

Pre-recorded videos are also available [here](#).

4 Subsessions

- **Enabling On-Device CNN Training by Self-Supervised Instance Filtering and Error Map Pruning**
🕒 11:45am - 12:25pm, Sep 23
- **DeepPrefetcher: A Deep Learning Framework for Data Prefetching in Flash Storage Devices**
🕒 11:45am - 12:25pm, Sep 23
- **WinDConv: A Fused Datapath CNN Accelerator for Power-efficient Edge Devices**
🕒 11:45am - 12:25pm, Sep 23
- **UltraTrail: A Configurable Ultra-Low Power TC-ResNet AI Accelerator for Efficient Keyword Spotting**
🕒 11:45am - 12:25pm, Sep 23

CODES+ISSS Session 6B: Memory and Scheduling

🕒 11:45am - 12:25pm, Sep 23

CODES+ISSS

Moderator: Zili Shao, *The Chinese University of Hong Kong*

Memory accesses, memory architectures, and scheduling play important roles in the performance of the embedded systems. This session explores the optimization for algorithms, memory architectures, virtual memory, thread migration, and task scheduling.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Shift-limited Sort: Optimizing Sorting Performance on Skyrmion Memory based Systems**
🕒 11:45am - 12:25pm, Sep 23
- **ReSQM: Accelerating Database Operations Using ReRAM-based Content Addressable Memory**
🕒 11:45am - 12:25pm, Sep 23
- **When Storage Response Time Catches Up with Overall Context Switch Overhead, What is Next?**
🕒 11:45am - 12:25pm, Sep 23
- **Hardware-Level Thread Migration to Reduce On-Chip Data Movement via Reinforcement Learning**
🕒 11:45am - 12:25pm, Sep 23
- **Runtime Task Scheduling using Imitation Learning for Heterogeneous Many-Core Systems**
🕒 11:45am - 12:25pm, Sep 23

EMSOFT Session 6C: Modeling and Verification

🕒 11:45am - 12:25pm, Sep 23

EMSOFT

Moderator: Ichiro Hasuo, *National Institute of Informatics, Japan*

Formal methods for synthesis and verification of discrete and continuous systems. Namely, (a) an

automated debugging methodology for Simulink models based on bug localization with Signal Temporal Logic and model repair with automated parameter tuning; (b) a method for mining a broad fragment of Shape Expressions from time-series data using techniques from linear regression, unsupervised clustering, and learning finite automata; (c) an algorithm for soundly synthesizing distributed systems based on iteratively building assumptions and guarantees at each process using reactive synthesis; (d) a formalism for online monitoring that relaxes the causality restriction of other approaches and is, for instance, suitable for monitoring physiological signals in medical devices; and (e) a model checking approach for finite-time safety verification of black-box continuous-time systems based on probably approximately correct learning.

Pre-recorded videos are also available [here](#).

5 Subsessions

- **Specification Guided Automated Debugging of CPS Models**
🕒 11:45am - 12:25pm, Sep 23
- **Mining Shape Expressions from Examples**
🕒 11:45am - 12:25pm, Sep 23
- **Assume-Guarantee Distributed Synthesis**
🕒 11:45am - 12:25pm, Sep 23
- **Online Signal Monitoring with Bounded Lag**
🕒 11:45am - 12:25pm, Sep 23
- **PAC Model Checking of Black-Box Continuous-Time Dynamical Systems**
🕒 11:45am - 12:25pm, Sep 23

12:30pm

Meet the Award Winners

🕒 12:30pm - 1:00pm, Sep 23

Plenary

CASES Networking

🕒 12:30pm - 1:00pm, Sep 23

CASES

CODES+ISSS Networking

🕒 12:30pm - 1:00pm, Sep 23

CODES+ISSS

EMSOFT Networking

🕒 12:30pm - 1:00pm, Sep 23

EMSOFT

Thu, Sep 24, 2020

8:15am

RSP Opening and Keynote

🕒 8:15am - 9:00am, Sep 24

RSP

The International Workshop on Rapid System Prototyping (RSP) emphasizes design experience sharing and collaborative approach between hardware and software research communities from industry and academy. It considers prototyping as an iterative design approach for embedded hardware and software systems. The RSP series of workshop aim at bridging the gaps in embedded system design between

applications, architectures, tools, and technologies to achieve rapid system prototyping of emerging software and hardware systems.

2 Subsessions

- **Welcome - Opening Remarks**
🕒 8:15am - 8:30am, Sep 24
- **Keynote: Quantizing neural networks for ultra-low-precision computation**
🕒 8:30am - 9:00am, Sep 24

9:00am

RSP Session A

🕒 9:00am - 9:30am, Sep 24

RSP

Session Chair: Sungjoo Yoo, Seoul National University

Pre-recorded videos are also available [here](#).

3 Subsessions

- **Hardware-in-the-loop simulation with dynamic partial FPGA reconfiguration applied to computer vision in ROS-based UAV**
🕒 9:00am - 9:30am, Sep 24
- **Advanced Debugging Architecture for Smart Inertial Sensors using Sensor-in-the-Loop**
🕒 9:00am - 9:30am, Sep 24
- **A combined fast/cycle accurate simulation tool for reconfigurable accelerator evaluation: application to distributed data management**
🕒 9:00am - 9:30am, Sep 24

AAIEA

🕒 9:00am - 5:00pm, Sep 24

AAIEA

[Workshop on Accelerating Artificial Intelligence for Embedded Autonomy \(AAIEA\)](#)

[The preliminary program has been posted on-line](#)

https://alessandro-pinto.github.io/aaiea2020/5_program/

This year, we are featuring a good mix of talks from industry and academia, and spanning theory and practice.

We are planning for a very interactive virtual workshop. If you are working in the area of intelligence at the edge, consider joining us for this interesting virtual session.

10:15 - 10:30

Introduction to the workshop

Workshop organizers

10:30 - 11:00

The Graphcore Intelligence Processing Unit - A new processor architecture for machine intelligence

Dr. George Mathew

AI Applications Specialist, Graphcore

11:00 - 11:30

Automated Design of Efficient Deep Neural Networks for the edge

Bichen Wu

University of California, Berkeley

11:30 - 12:00

Analog resistive crossbar arrays for deep learning acceleration

Dr. Martin M. Frank

IBM T.J. Watson Research Center

12:00 - 13:00

Lunch break

13:00 - 13:45 : **Keynote**

Human-Centric Computing

Jan M. Rabaey

Donald O. Pederson Distinguished Professor, EECS Department, University of California, Berkeley

13:45 - 14:00

Break

14:00 - 14:30

Implementing Deep Learning on a Small UAS for an ISR Mission

Dr. Arjuna Flenner

Senior Technical Leader – AI & Image Processing, Advanced & Special Programs, GE Aviation Systems

14:30 - 15:00

Autonomy at the Edge: Ultra-Low Power Hardware Design for Intelligent Micro-robotics

Arijit Raychowdhury

Professor, Electrical and Computer Engineering, Georgia Institute of Technology

15:00 - 15:30

Real-time Motion Planning for the Masses

Dan Sorin

Addy Professor of Electrical and Computer Engineering and of Computer Science, Duke University

15:30 - 16:00 : Concluding Remarks and next steps

Enabling the Future of Embedded Autonomy

1 Subsessions

● Invited Talks

🕒 10:15am - 4:00pm, Sep 24

MSC

🕒 9:00am - 5:00pm, Sep 24

MSC

[International Workshop on Memory and Storage Computing \(MSC\)](#)

MSC will start at Beijing time (Sept. 24, 9:00am-17:00pm).

<https://zoom.com.cn/j/91561647801?pwd=eVU1MDJrNEpETE9zcE9lNmQrQ2tEQT09>

Password: 0924

Program:

Time	Session	Speakers and Dept
Session Chair: Liang Shi		
09:00-10:00	KEYNOTES	Li Jiang, Shanghai Jiaotong U
Session Chair: Yuan-hao Chang		
10:00-10:20	One-Memory Computer System: When the Line Between Main Memory and Storage is Blurred via NVRAM	Shuo-Han Chen, National Taipei University of Technology
10:20-10:40	Toward Instantaneous Sanitization through Disturbance-induced Errors and Recycling Programming over 3D Flash Memory	Chien-Chung Ho, National Chung Cheng University
10:40-11:00	How to cultivate a green decision tree without loss of accuracy?	Tseng-Yi Chen, National Central University
11:00-11:20	Exploring the Memory Heterogeneity for Performance Tuning	Che-Wei Chang, Chang Gung University
11:20-11:40	Scalable, Efficient, and Compact Frequent-Pattern Mining on Nonvolatile Memories	Po-Chun Huang, National Taipei University of Technology
Session Chair: Chien-Chun Ho		
13:30-14:10	Invited talk	Ning Zheng, Scaflux
Session Chair: Congming Gao		
14:10-16:00	Invited Presentation	Feng Wang, Peking University Xiangzhong Luo, NTU He Zhang, BUAA Hui Sun, Anhui University
Session Chair: Weilan Wang		
16:00-17:00	Presentation Papers	Mingyue Liu, SEU Chongnan Ye, ShanghaiTech university Min Jia, ECNU

5 Subsessions

- **keynote: ReRAM-based In-Memory Computing – an algorithm –architecture co-design approach towards the POS/w era**
⌚ 9:00am - 10:00am, Sep 24
- **Invited Session 1**
⌚ 10:00am - 12:00pm, Sep 24
- **Invited Talk: How computational storage could benefit database applications**
⌚ 1:00pm - 2:00pm, Sep 24
- **Invited Session 2**
⌚ 2:00pm - 4:00pm, Sep 24
- **Paper Presentation**
⌚ 4:00pm - 5:00pm, Sep 24

NOCS - Opening Remarks & Keynote I

⌚ 9:00am - 10:10am, Sep 24

NOCS

3 Subsessions

- **Opening Remarks**

🕒 9:00am - 9:05am, Sep 24

● **Keynote I: "Network Congestion: Analysis and Effective Solutions for Datacenters"**

🕒 9:05am - 10:05am, Sep 24

● **Break**

🕒 10:05am - 10:10am, Sep 24

9:40am

RSP Session B

🕒 9:40am - 10:10am, Sep 24

RSP

Session Chair: Kenneth Kent, University of New Brunswick

Pre-recorded videos are also available [here](#).

3 Subsessions

● **Mathematic models based on multiple-criteria decision analysis for tuning industrial CNN in an FPGA computing cluster**

🕒 9:40am - 10:10am, Sep 24

● **MPSoC Fast Prototyping of a Reconfigurable DU Downlink Transmission Chain for 5G New Radio**

🕒 9:40am - 10:10am, Sep 24

● **FPGA based design and prototyping of efficient 5G QC-LDPC channel decoding**

🕒 9:40am - 10:10am, Sep 24

10:00am

HENP

🕒 10:00am - 12:30pm, Sep 24

HENP

International Workshop on Highly Efficient Neural Processing (HENP)

<http://cmalab.snu.ac.kr/HENP2020>

<https://acm-org.zoom.us/j/99050284189?pwd=eXM3VE00UGxBb0pOa29HVINWNGdxQT09>

The International Workshop on Highly Efficient Neural Processing is a forum for presentations of state-of-the-art research in highly efficient neural processing. This year's online workshop consists of invited oral presentations from Amazon, UC Berkeley, Facebook, Furiosa AI, and SNU.

- "Furiosa Renegade: the next-generation high performance AI chip for data center," Dr. June Paik, Furiosa AI
- "Position-based Scaled Gradient for Model Quantization," Prof. Nojun Kwak, Seoul National University
- "Moving Big Cloud Applications to the Edge: NLP and Recommendation Systems," Prof. Kurt Keutzer, University of California, Berkeley
- "Accelerating the Pace of AWS Inferentia Chip Development, From Concept to End Customers Use," Dr. Randy Huang, Amazon Web Services
- "Efficient Audio-Visual Understanding on AR Devices," Dr. Vikas Chandra, Facebook

1 Subsessions

● **Invited talks**

🕒 10:00am - 12:30pm, Sep 24

10:10am

NOCS - Regular Paper Session A: "Architecture & RDMA"

🕒 10:10am - 11:30am, Sep 24

NOCS

Regular Paper Session A: "Architecture & RDMA"

Mirror for Chinese viewers: <https://www.bilibili.com/video/BV17k4y1y7E1>

5 Subsessions

- **In-Network Memory Access Ordering for Heterogeneous Multicore Systems**
🕒 10:10am - 10:30am, Sep 24
- **Scheduled Deflections for Resilient Bufferless Networks-on-Chip**
🕒 10:30am - 10:45am, Sep 24
- **Combinatorics and Geometry of Memory Access Structures for the Many-ported, Distributed and Shared Memory Architecture**
🕒 10:45am - 11:00am, Sep 24
- **PART: Pinning Avoidance in RDMA Technologies**
🕒 11:00am - 11:20am, Sep 24
- **Break**
🕒 11:20am - 11:30am, Sep 24

10:20am

RSP Session C

🕒 10:20am - 10:50am, Sep 24

RSP

Session Chair: Amer Baghdadi, IMT Atlantique/Lab-STICC

Pre-recorded videos are also available [here](#).

3 Subsessions

- **(System)Verilog to Chisel Translation for Faster Hardware Design**
🕒 10:20am - 10:50am, Sep 24
- **NestedNet: A Container-based Prototyping Tool for Hierarchical Software Defined Networks**
🕒 10:20am - 10:50am, Sep 24
- **Desired Footprint by Technology Mapping Modification using a Genetic Algorithm in Odin II**
🕒 10:20am - 10:50am, Sep 24

11:30am

NOCS - Special Session A: "Unlock the NoC: Transforming NoC Research with Physical Design Awareness" Session Chairs: Chris Batten (Cornell) and Michael Taylor (University of Washington)

🕒 11:30am - 1:00pm, Sep 24

NOCS

Special Session A: "Unlock the NoC: Transforming NoC Research with Physical Design Awareness"

Session Chairs: Chris Batten (Cornell) and Michael Taylor (University of Washington)

Overview

Chris Batten (Cornell) and Michael Taylor (University of Washington)

Ruche Networks: Wire-Maximal, No-Fuss NoCs

Dai Cheol Jung, Scott Davidson, Chun Zhao, Dustin Richmond and Michael Bedford Taylor (University of Washington)

Implementing Low-Diameter On-Chip Networks Using a Tiled Physical Design Methodology

Yanghui Ou, Shady Agwa, Christopher Batten (Cornell University)

NoC Symbiosis

Daniel Petrisko, Chun Zhao, Scott Davidson, Paul Gao, Dustin Richmond and Michael Bedford Taylor (University of Washington)

3 Subsessions

- **Ruche Networks: Wire-Maximal, No-Fuss NoCs**
🕒 11:30am - 12:00pm, Sep 24
- **Implementing Low-Diameter On-Chip Networks Using a Tiled Physical Design Methodology**
🕒 12:00pm - 12:30pm, Sep 24
- **NoC Symbiosis**
🕒 12:30pm - 1:00pm, Sep 24

Fri, Sep 25, 2020

9:00am

NOCS - Regular Paper Session B: "Multicast & Security"

🕒 9:00am - 10:10am, Sep 25

NOCS

Regular Paper Session B: "Multicast & Security"

Session Chair: TBD

Mirror for Chinese viewers: <https://www.bilibili.com/video/BV1th411R794>

(L) An Efficient Multicast Router using Shared-Buffer with Packet Merging for Dataflow Architecture

Yi Li, Meng Wu, Xiaochun Ye, Wenming Li and Dongrui Fan

(L) SecONet: A Security Framework for a Photonic Network-on-Chip

Janibul Bashir, Chandran Goodchild and Smruti R. Sarangi

(L) SECTAR: Secure NoC using Trojan Aware Routing

Manju R, Abhijit Das, John Jose and Prabhat Mishra

4 Subsessions

- **An Efficient Multicast Router using Shared-Buffer with Packet Merging for Dataflow Architecture**
🕒 9:00am - 9:20am, Sep 25
- **SecONet: A Security Framework for a Photonic Network-on-Chip**
🕒 9:20am - 9:40am, Sep 25

- **SECTAR: Secure NoC using Trojan Aware Routing**

🕒 9:40am - 10:00am, Sep 25

- **Break**

🕒 10:00am - 10:10am, Sep 25

10:10am

NOCS - Keynote II: "Domain-Specific Networks for Machine Learning"

🕒 10:10am - 11:20am, Sep 25

NOCS

Keynote II: "Domain-Specific Networks for Machine Learning"

Speaker: Dennis Abts (Groq)

Session Chair: John Kim (KAIST)

2 Subsessions

- **Keynote II: "Domain-Specific Networks for Machine Learning"**

🕒 10:10am - 11:10am, Sep 25

- **Break**

🕒 11:10am - 11:20am, Sep 25

11:20am

NOCS - Regular Paper Session C: "Technology in Communication"

🕒 11:20am - 12:00pm, Sep 25

NOCS

Regular Paper Session C: "Technology in Communication"

Session Chair: TBD

Mirror for Chinese viewers: <https://www.bilibili.com/video/BV1hk4y1y7F8>

(L) PROTEUS: Rule-Based Self-Adaptation in Photonic NoCs for Loss-Aware Dynamic Co-Optimization of Performance and Laser Power

Sairam Sri Vatsavai, Venkata Sai Praneeth Karempudi and Ishan Thakkar

(S) Improving Inference Latency and Energy of DNNs through Wireless Enabled Multi Chip-Module-based Architectures and Model Parameters Compression

Maurizio Palesi, Giuseppe Ascia, Davide Patti, Salvatore Monteleone, Vincenzo Catania and Andrea Mineo

3 Subsessions

- **PROTEUS: Rule-Based Self-Adaptation in Photonic NoCs for Loss-Aware Dynamic Co-Optimization of Performance and Laser Power**

🕒 11:20am - 11:40am, Sep 25

- **Improving Inference Latency and Energy of DNNs through Wireless Enabled Multi Chip-Module-based Architectures and Model Parameters Compression**

🕒 11:40am - 11:55am, Sep 25

- **Break**

🕒 11:55am - 12:00pm, Sep 25

12:00pm

NOCS - Special Session B: "Scalable Platforms for Machine Learning: An Industry Perspective"

🕒 12:00pm - 1:30pm, Sep 25

NOCS

Special Session B: "Scalable Platforms for Machine Learning: An Industry Perspective"

Session Chair: TBD

Accelerating the Network for Deep Learning at Scale

Benjamin Klenk (NVIDIA)

The Wafer Scale Interconnect in the Wafer Scale Engine

Robert Hesse (Cerebras)

2 Subsessions

- **Accelerating the Network for Deep Learning at Scale**
🕒 12:00pm - 12:45pm, Sep 25
- **The Wafer Scale Interconnect in the Wafer Scale Engine**
🕒 12:45pm - 1:30pm, Sep 25