Embedded Systems Week 2012

7th – 12th October 2012, Tampere Hall, Tampere, Finland

www.esweek.org

ESWEEK AT A GLANCE

Oct. 7 (SUN)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0930		EMSOFT Tutorial 1	CASES Tutorial 1	CODES+ISSS Tutorial 1	CASA	MeCoES	EON
0930-1000		**Coffee Break (Room Rondo)**					
1000-1200		EMSOFT Tutorial 1	CASES Tutorial 1	CODES+ISSS Tutorial 1	CASA	MeCoES	EON
1200-1300		**Lunch (Tampere Hall Restaurant)**					
1300-1500		EMSOFT Tutorial 2	CASES Tutorial 2	CODES+ISSS Tutorial 2	CASA	MeCoES	EON
1500-1530		**Coffee Break (Room Rondo)**					
1530-1730		EMSOFT Tutorial 2	CASES Tutorial 2	CODES+ISSS Tutorial 2	CASA	MeCoES	EON
1800-1930		**Welcome Reception (Museum Center Vapriikki)**					

Oct. 8 (MON)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0830	Opening Remarks						
0830-0930	Keynote by Hannu Kauppinen, Nokia						
0930-1000	**Coffee Break (Room Rondo)**						
1000-1200	EMSOFT Session 1A	CASES Session 1	EMSOFT Session 1B	CODES+ISSS Session 1A	CODES+ISSS Session 1B		
1200-1300	**Lunch (Tampere Hall Restaurant)**						
1300-1500	EMSOFT Session 2A	CASES Session 2	EMSOFT Session 2B	CODES+ISSS Session 2A	CODES+ISSS Session 2B		
1500-1530	**Coffee Break (Room Rondo)**						
1530-1730		CASES Session 3	EMSOFT Session 3	CODES+ISSS Session 3A	CODES+ISSS Session 3B		
1830-2030	**ESWeek Organizing Committee and TPC Meeting (Restaurant Finlaysonin Palatsi)**						

Oct. 9 (TUE)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0830-0930	Keynote by Satnam Singh, Google						
0930-1000	**Coffee Break (Room Rondo)**						
1000-1200		CASES Session 4	EMSOFT Session 4	CODES+ISSS Session 4A	CODES+ISSS Session 4B		
1200-1300	**Lunch (Tampere Hall Restaurant)**						
1300-1500	Industrial Session 1	CASES Session 5	EMSOFT Session 5	CODES+ISSS Session 5A	CODES+ISSS Session 5B		
1500-1530	**Coffee Break (Room Rondo)**						
1530-1730	CODES+ISSS Session 6A	CASES Session 6	EMSOFT Session 6	CODES+ISSS Session 6B	CODES+ISSS Session 6C		
1830-2030	**Banquet Gala (Restaurant Scandic Rosendahl)**						

Oct. 10 (WED)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0830-0930	Keynote by Jong Choi, Samsung						
0930-1000	**Coffee Break (Room Rondo)**						
1000-1200	Industrial Session 2	CASES+CODES+ISSS Session 7	EMSOFT Session 7	CODES+ISSS Session 7A	CODES+ISSS Session 7B		
1200-1300	**Lunch (Tampere Hall Restaurant)**						
1300-1500	Industrial Session 3	CASES+CODES+ISSS Session 8	EMSOFT Session 8	CODES+ISSS Session 8A	CODES+ISSS Session 8B		
1500-1530	**Coffee Break (Room Rondo)**						
1530-1730	Industrial Panel						
1730-1745	Best paper award Announcements Closing remarks						

Oct. 11 (THU)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0800-0900		RSP	ESTIMedia		MeAOW	WESE	WESS
0900-0930		**Coffee Break (Room Rondo)**					
0930-1130		RSP	ESTIMedia		MeAOW	WESE	WESS
1130-1300		**Lunch (Tampere Hall Restaurant)**					
1300-1500		RSP	ESTIMedia		MeAOW	WESE	WESS
1500-1530		**Coffee Break (Room Rondo)**					
1530-1730		RSP	ESTIMedia		MeAOW	WESE	WESS

Oct. 12 (FRI)	Pieni Sali	Sopraano	Sonaatti 1	Studio	Sonaatti 2	Opus 4	Aaria
0830-0930		RSP	ESTIMedia				
0930-1000		**Coffee Break (Room Rondo)**					
1000-1200		RSP	ESTIMedia				

MONDAY 8th OCTOBER

CASES	EMSOFT	CODES+ISSS
Opening remarks		
Keynote speech by Hannu Kauppinen, Nokia: Wireless Innovations for Smartphones		
Session 1: Security in Memory *Session chair: Heiko Falk* **1.1 Side Channel Attacks and the Non Volatile Memory of the Future** *Zoya Dyka, Christian Walcyk, Christian Wenger and Peter Langendoerfer* **1.2 Static Secure Page Allocation for Light-Weight Dynamic Information Flow Tracking** *Juan Carlos Martinez Santos, Yunsi Fei and Zhijie Jerry Shi* ★ **1.3 A Cost-Effective Tag Design for Memory Data Authentication in Embedded Systems** *Mei Hong, Hui Guo and X. Sharon Hu*	**Session 1A: Testing and Characterization of Embedded Software** **1A.1 Debugging Embedded Multimedia Application Traces Through Periodic Pattern Mining** *Patricia Lopez Cueva, Aurelie Bertaux, Alexandre Termier, Jean Francois Mehaut and Miguel Santana* **1A.2 Smart Layers and Dumb Result: IO Characterization of an Android-Based Smartphone** *Kisung Lee and Youjip Won* **1A.3 Xemu: An Efficient Qemu Based Binary Mutation Testing Framework for Embedded Software** *Markus Becker, Daniel Baldin, Christoph Kuznik, Mabel Mary Joy, Tao Xie and Wolfgang Mueller* **Session 1B: Theoretical Aspects of Embedded Systems** **1B.1 Finite Automata with Time-Delay Blocks** *Krishnendu Chatterjee, Thomas Henzinger and Vinayak Prabhu* ★ **1B.2 Synthesis from Incompatible Specifications** *Pavol Cerny, Sivakanth Gopi, Thomas A. Henzinger, Arjun Radhakrishna and Nishant Totla* **1B.3 Timed Model Checking with Abstractions: Towards Worst-Case Response Time Analysis in Resource-Sharing Manycore Systems** *Georgia Giannopoulou, Kai Lampka, Nikolay Stoimenov and Lothar Thiele*	**Session 1A: Software Solutions for Handling Physical Effects in Embedded Platforms** *Session chair: Karam S. Chatha* ★ **1A.1 A Real-Time, Energy-Efficient System Software Suite for Heterogeneous Multicore Platforms** *Shih-Hao Hung, Chi-Sheng Shih, Tei-Wei Kuo, Chia-Heng Tu and Che-Wei Chang* **1A.2 Lifetime Improvement through Runtime Wear-based Task Mapping** *Adam Hartman and Donald Thomas* **1A.3 ViPZonE: OS-Level Memory Variability-Driven Physical Address Zoning for Energy Savings** *Luis Bathen, Mark Gottscho, Nikil Dutt, Puneet Gupta and Alex Nicolau* **Session 1B: Robust Embedded Architecture** *Session chair: José L. Ayala* **1B.1 Dynamic Transient Fault Detection and Recovery for Embedded Processor Datapaths** *Garo Bournoutian and Alex Orailoglu* **1B.2 SPI-SNOOPER: A Hardware-Software Approach for Transparent Network Monitoring in Wireless Embedded Systems** *Mohammad Hossain, Woo Suk Lee and Vijay Raghunathan* **1B.3 A Novel NoC–based Design for Fault-tolerance of Last-level Caches in CMPs** *Abbas BanaiyanMofrad, Gustavo Girão and Nikil Dutt*
Session 2: Static and Dynamic Compilation Techniques *Session chair: Aviral Shrivastava* **2.1 From Sequential Programming to Flexible Parallel Execution** *Arun Raman, David I. August and Jae W. Lee* **2.2 A Hybrid Just-In-Time Compiler for Android** *Guillermo A. Perez, Yeh-Ching Chung, Chung-Min Kao and Wei-Chung Hsu* **2.3 LLBT: An LLVM-based Static Binary Translator** *Bor-Yeh Shen, Jiunn-Yeu Chen, Wei-Chung Hsu and Wuu Yang*	**Session 2A: Operating Systems** **2A.1 Server-Based Scheduling of Parallel Real-Time Tasks** *Luis Nogueira and Luis Miguel Pinho* **2A.2 Operating System Support for Redundant Multithreading** *Björn Döbel, Hermann Härtig and Michael Engel* **2A.3 Flattening Hierarchical Scheduling** *Adam Lackorzynski, Alexander Warg, Marcus Völp and Hermann Härtig* **Session 2B: Control Theory** **2B.1 Trigger Memoization in Self-Triggered Control** *Indranil Saha and Rupak Majumdar* **2B.2 Feedback Thermal Control of Real-Time Systems on Multicore Processors** *Yong Fu, Chenyang Lu, Nicholas Kottenstette and Xenofon Koutsoukos* ★ **2B.3 Synthesis of Minimal Error Control Software** *Rupak Majumdar, Indranil Saha and Majid Zamani*	**Session 2A: Managing Parallelism in Multi-core Systems** *Session chair: Rolf Ernst* **2A.1 Automatic Extraction of Multi-Objective Aware Pipeline Parallelism Using Genetic Algorithms** *Daniel Cordes, Michael Engel, Peter Marwedel and Olaf Neugebauer* **2A.2 Managing Latency in Embedded Streaming Applications under Hard-Real-Time Scheduling** *Mohamed Bamakhrama and Todor Stefanov* **2A.3 Dynamic Scheduling of Stream Programs on Embedded Multi-core Processors** *Haeseung Lee, Weijia Che and Karam Chatha* **Session 2B: NOC and Memory Performance Analysis and Mapping** *Session chair: Jari Nurmi* ★ **2B.1 A Distributed Interleaving Scheme for Efficient Access to WideIO DRAM Memory** *Ciprian Seiculescu, Luca Benini and Giovanni De Micheli* **2B.2 Minimizing Power Supply Noise Through Harmonic Mappings in Networks-on-Chip** *Nizar Dahir, Terrence Mak, Fei Xia and Alex Yakovlev* **2B.3 Worst-case Performance Analysis of 2-D Mesh NoCs using Multi-path Minimal Routing** *Gaoming Du, Cunqiang Zhang, Zhonghai Lu, Alberto Saggio and Minglun Gao*
Session 3: Optimizing Heterogeneous Multicore Systems *Session chair: Brett Meyer* ★ **3.1 Power Agnostic Technique for Efficient Temperature Estimation of Multicore Embedded Systems** *Devendra Rai, Hoeseok Yang, Iuliana Bacivarov and Lothar Thiele* **3.2 Scenario-Based Design Flow for Mapping Streaming Applications onto On-Chip Many-Core Systems** *Lars Schor, Iuliana Bacivarov, Devendra Rai, Hoeseok Yang, Shin-haeng Kang and Lothar Thiele* **3.3 RACECAR: A Heuristic for Automatic Function Specialization on Multi-core Heterogeneous Systems** *John Wernsing, Greg Stitt and Jeremy Fowers*	**Session 3: Hardware Support** **3.1 Hardware Data Structures for Hard Real-Time Systems** *Gedare Bloom, Gabriel Parmer, Bhagirath Narahari and Rahul Simha* **3.2 A Low-Overhead Dedicated Execution Support For Stream Applications On Shared-Memory CMP** *Paul Dubrulle, Stéphane Louise, Renaud Sirdey and Vincent David* **3.3 Partitioned Scheduling for Real-Time Tasks on Multiprocessor Embedded Systems with Programmable Shared SRAMS** *Che-Wei Chang, Jian-Jia Chen, Waqaas Munawar, Tei-Wei Kuo and Heiko Falk*	**Session 3A: Efficient Simulation Techniques** *Session chair: Mingsong Chen* **3A.1 HyCoS: Hybrid Compiled Simulation of Embedded Software with Target Dependent Code** *Zhonglei Wang and Joerg Henkel* **3A.2 Fast simulation of systems embedding VLIW processors** *Luc Michel, Nicolas Fournel and Frédéric Pétrot* **3A.3 DIMSim: A Rapid Two-level Cache Simulation Approach for Deadline-based MPSoCs** *Mohammad Shihabul Haque, Roshan Ragel, Angelo Ambrose, Swarnalatha Radhakrishnan and Sri Parameswaran* **Session 3B: Routing Algorithms and NoC Architectures for Next-Generation 2D/3D SoCs** *Session chair: Zhonghai Lu* **3B.1 The Roce-Bush Router: A Case for Routing-centric Dimensional Decomposition for Low-latency 3D NoC Routers** *Miguel Salas and Sudeep Pasricha* **3B.2 Non-Intrusive Trace & Debug NoC Architecture with Accurate Timestamping for GALS SoCs** *Vladimir Todorov, Alberto Ghiribaldi, Helmut Reinig, Davide Bertozzi and Ulf Schlichtmann* ★ **3B.3 An Efficient Adaptive Routing Algorithm on a Highly Reconfigurable Network-on-Chip Architecture** *Zhiliang Qian, Paul Bogdan, Chi-Ying Tsui, Radu Marculescu and Guopeng Wei*

TUESDAY 9th OCTOBER

CASES	EMSOFT	CODES+ISSS
Keynote speech by Satnam Singh, Google: Computing Without Processors		

Session 4: Frontline Challenges in Versatile Computing *Session chair: Muhammad Shafique* **4.1 SiblingRivalry: Online Autotuning Through Local Competitions** *Jason Ansel, Maciej Pacula, Yee Lok Wong, Cy Chan, Marek Olszewski, Una-May O'Reilly and Saman Amarasinghe* **4.2 Function Inlining and Loop Unrolling for Loop Acceleration in Reconfigurable Processors** *Narasinga Rao Miniskar, Pankaj Shailendra Gode and Soma Kohli* **4.3 A Low-Overhead Interconnect Architecture for Virtual Reconfigurable Fabrics** *Aaron Landy and Greg Stitt*	**Session 4: Invited Session – Code-Level Timing Analysis** **4.1 Timing Analysis for Multicore/Manycore Architectures** *Kevin Hammond* **4.2 Reconciling Compilation and Timing Analysis** *Heiko Falk* **4.3 Early-Stage and Portable Timing Analysis** *Stefan M. Petters* **4.4 Analysis of Mixed-Critical Embedded Systems with Multiple Objectives** *Kim G. Larsen* **4.5 TACLe - An EU COST Action on Timing Analysis on Code-Level** *Björn Lisper*	**Session 4A: Advanced Simulation Techniques for Simulation-Based Validation** *Session chair: Frederic Petrot* ★ **4A.1 Dynamic Property Mining for Embedded Software** *Marco Bonato, Giuseppe Di Guglielmo, Masahiro Fujita, Franco Fummi and Graziano Pravadelli* **4A.2 Efficient Self-Learning Techniques for SAT-Based Test Generation** *Ang Li and Mingsong Chen* **4A.3 Using Static Analysis for Coverage Extraction from Emulation/Prototyping Platforms** *Viraj Athavale, Sam Hertz, Darshan Jetly, Vijay Ganesan, Jim Krysl and Shobha Vasudevan* **Session 4B: Emulation of Physical Systems and Design of Wireless Sensor Networks** *Session chair: Petru Eles* **4B.1 Synthesis of custom networks of heterogeneous processing elements for complex physical system emulation** *Chen Huang, Bailey Miller, Frank Vahid and Tony Givargis* **4B.2 Knowledge-Based Design Space Exploration of Wireless Sensor Networks** *Paolo Roberto Grassi, Ivan Beretta, Vincenzo Rana, Donatella Sciuto and David Atienza* **4B.3 Spatially- and Temporally-Adaptive Communication Protocols for Zero-Maintenance Sensor Networks Relying on Opportunistic Energy Scavenging** *Xuejing He, Robert Dick and Russ Joseph*
Session 5: Static and Dynamic Energy Management *Session chair: Henri-Pierre Charles* **5.1 Energy Efficient Hybrid Display and Predictive Models for Embedded and Mobile Systems** *Yuanfeng Wen, Ziyi Liu, Weidong Shi, Yifei Jiang, Albert Cheng and Khoa Le* ★ **5.2 Energy Efficient Special Instruction Support in an Embedded Processor with Compact ISA** *Dongrui She, Yifan He and Henk Corporaal* **5.3 When Less Is MOre (LIMO): Controlled Parallelism for Improved Energy Efficiency** *Gaurav Chadha, Satish Narayanasamy and Scott Mahlke*	**Session 5: Timing Analysis** **5.1 Estimation of Probabilistic Bounds on Phase CPI and Relevance in WCET Analysis** *Archana Ravindar and Srikant Y. N.* **5.2 Assessing the Suitability of the NGMP Multi-Core Processor in the Space Domain** *Mikel Fernandez, Roberto Gioiosa, Eduardo Quiñones, Luca Fossati, Marco Zulianello and Francisco J. Cazorla* **5.3 Compositional Temporal Analysis Model for Incremental Hard Real-Time System Design** *Joost Hausmans, Stefan Geuns, Maarten Wiggers and Marco Bekooij*	**Session 5A: Advances in Power/thermal optimization** *Session chair: Tohru Ishihara* ★ **5A.1 Performance Enhancement under Power Constraints using Heterogeneous CMOS-TFET Multicores** *Emre Kultursay, Karthik Swaminathan, Vinay Saripalli, Vijaykrishnan Narayanan, Mahmut Kandemir and Suman Datta* **5A.2 COOL: Control-based Optimization Of Load-balancing for Thermal Behavior** *Thomas Ebi, Hussam Amrouch and Jörg Henkel* **5A.3 Adaptive Online Heuristic Performance Estimation and Power Optimization for Reconfigurable Embedded Systems** *Jingqing Mu and Roman Lysecky* **Session 5B: Enabling hardware design in system context** *Session chair: Jarmo Takala* **5B.1 BPR: Fast FPGA Placement and Routing Using Macroblocks** *James Coole and Greg Stitt* **5B.2 Generating Interlocked Instruction Pipelines from Specifications of Instruction Sets** *Ralf Dreesen* **5B.3 Designing parameterized signal processing IPs for high level synthesis in a model based design environment** *Shahzad Ahmad Butt and Luciano Lavagno*
Session 6: Software/Hardware Techniques for Cache Management *Session chair: Oliver Bringmann* **6.1 Lazy Cache Invalidation for Self-Modifying Codes** *Anthony Gutierrez, Joseph Pusdesris, Ronald Dreslinski and Trevor Mudge* **6.2 Static Task Partitioning for Locked Caches in Multi-Core Real-Time Systems** *Abhik Sarkar, Frank Mueller and Harini Ramaprasad* **6.3 Revisiting Level-0 Caches in Embedded Processors** *Nam Duong, Taesu Kim, Dali Zhao and Alex Veidenbaum*	**Session 6: Special Session: An Overview Of The Career of Paul Caspi** Speakers: *Edward A. Lee, Stavros Tripakis, Albert Benveniste, Marc Pouzet, Florence Maraninchi*	**Session 6A: Testbenches for Advanced TLM Verification** *Session chair: Wolfgang Mueller* **6A.1 SystemC as A Completing Pillar in Industrial UVM Based Verification Environments** *Wolfgang Ecker, Volkan Esen, Tudor Timisescu and Andreas v. Schwerin* **6A.2 The System Verification Methodology for Advanced TLM Verification** *Christoph Kuznik, Marcio Oliviera, Wolfgang Müller, Finn Haedicke, Hoang Le, Daniel Grosse, Rolf Drechsler, Wolfgang Ecker, and Volkan Esen* **6A.3 Generation of TLM Testbenches using Mutation Testing** *Marcelo Sousa and Alper Sen* **6A.4 A Testbench Specification Language for SystemC Verification** *Graziano Pravadelli and Giuseppe Di Guglielmo* **6A.5 SystemC simulation on GP-GPUs: CUDA vs. OpenCL** *Nicola Bombieri, Sara Vinco, Valeria Bertacco and Debapriya Chatterjee* **Session 6B: Power-Efficient Mobile Computing** *Session chair: William Fornaciari* **6B.1 DevScope: A Nonintrusive and Online Power Analysis Tool for Smartphone Hardware Components** *Wonwoo Jung, Chulkoo Kang, Chanmin Yoon, Dongwon Kim and Hojung Cha* **6B.2 ADEL: An Automatic Detector of Energy Leaks for Smartphone Applications** *Lide Zhang, Mark Gordon, Robert Dick, Morley Mao, Perter Dinda and Lei Yang* **6B.3 Don't burn your mobile! Safe Computational Re-Sprinting via Model Predictive Control** *Andrea Tilli, Andrea Bartolini, Matteo Cacciari and Luca Benini* **Session 6C: System-level synthesis and optimization** *Session chair: Brett Meyer* **6C.1 Concurrent Architecture and Schedule Optimization of Time-triggered Automotive Systems** *Martin Lukasiewycz and Samarjit Chakraborty* **6C.2 A SAFE Approach towards Early Design Space Exploration of Fault-tolerant Multimedia MPSoCs** *Peter van Stralen and Andy Pimentel* **6C.3 Synthesis of Optimized Hardware Transactors from Abstract Communication Specifications** *Dongwook Lee, Hyungman Park and Andreas Gerstlauer*

WEDNESDAY 10th OCTOBER

Joint CASES & CODES+ISSS	EMSOFT	CODES+ISSS
Keynote speech by Jong Choi, Samsung: A Standards-Based, Fully-Open Software Platform for Smart Embedded Systems		
Session 7: New Advances in Microfluidic Chips *Session chair: Fadi Kurdahi* **7.1 Fast Online Synthesis of Generally Programmable Digital Microfluidic Biochips** *Daniel Grissom and Philip Brisk*	**Session 7: Languages, Formal Models and Algorithms (1)** ★ **7.1 Programming Parallelism with Futures in Lustre** *Albert Cohen, Leonard Gerard and Marc Pouzet* **7.2 Towards Network-On-Chip Agreement Protocols** *Borislav Nikolic and Stefan Petters*	**Session 7A: Power, Reliability, and Security Issues from Systems to Circuits** *Session chair: Vijaykrishnan Narayanan* **7A.1 Enabling Ultra-Low Power Operation in High-End Wireless Sensor Networks Nodes** *Carlo Brandolese, William Fornaciari, Luigi Rucco and Federico Terraneo* **7A.2 Reducing NBTI-induced Processor Wearout by Exploiting the Timing Slack of Instructions** *Fabian Oboril, Farshad Firouzi, Saman Kiamehr and Mehdi Tahoori*

7.2 An intelligent compaction technique for pin constrained routing in Cross referencing Digital microfluidic biochips *Pranab Roy, Sudipta Chakraborty, Modud Sohid, Hafizur Rahaman, Parthasarathi Dasgupta and Rupam Bhattacharya* **7.3 Architectural Synthesis of Flow-Based Microfluidic Large-Scale Integration Biochips** *Wajid Hassan Minhass, Paul Pop, Jan Madsen and Felician Blaga*	**7.3 Input-Output Stability for Discrete Systems** *Paulo Tabuada, Ayca Balkan, Sina Yamac Caliskan, Yasser Shoukry and Rupak Majumdar*	**7A.3 LRCG: Latch-based Random Clock-Gating for Preventing Power Analysis Side-Channel Attacks** *Kazuyuki Tanimura and Nikil Dutt* **Session 7B: Real-time and Mixed Critical Systems** *Session chair: Todor Stefanov* **7B.1 Worst-Case Throughput Analysis of Real-Time Dynamic Streaming Applications** *Firew Siyoum, Marc Geilen, Orlando Moreira and Henk Corporaal* **7B.2 Synthesis of Communication Schedules for TTEthernet-based Mixed-Criticality Systems** *Domitian Tamas-Selicean, Paul Pop and Wilfried Steiner* **7B.3 A Hierarchical Control Scheme for Energy Quota Distribution in Hybrid Distributed Video Coding** *Muhammad Usman Karim Khan, Muhammad Shafique and Jörg Henkel*
Session 8: Memory management *Session chair: Frank Mueller* **8.1 DaaC: Device-reserved Memory as an Eviction-based File Cache** *Jinkyu Jeong, Hwanju Kim, Jeaho Hwang, Joonwon Lee and Seungryoul Maeng* **8.2 Integrating Software Caches with Scratch Pad Memory** *Prasenjit Chakraborty and Preeti Ranjan Panda* **8.3 Working-Set-Based Address Mapping for Ultra-Large-Scaled Flash Devices** *Ming-Chang Yang, Yuan-Hao Chang, Po-Chun Huang and Tei-Wei Kuo*	**Session 8: Languages, Formal Models and Algorithms (2)** **8.1 On Model Based Synthesis of Embedded Control Software** *Vadim Alimguzhin, Federico Mari, Igor Melatti, Ivano Salvo and Enrico Tronci* **8.2 A New Data Flow Analysis Model For TDM** *Alok Lele, Orlando Moreira and Pieter Cuijpers*	**Session 8A: Co-design in the real world** *Session chair: Claudio Brunelli* **8A.1 An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to an Industrial Multi-Cluster Architecture** *Edoardo Paone, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, Diego Melpignano, Germain Haugou and Thierry Lepley* **8A.2 A Case of System-level Hardware/Software Co-design and Co-verification of a Commodity Multi-Processor System with Custom Hardware** *Sungpack Hong, Tayo Oguntebi, Jared Casper, Nathan Bronson, Christos Kozyrakis and Kunle Olukotun* **8A.3 A Configurable Test Infrastructure using a Mixed-Language and Mixed-Level IP Integration IP-XACT Flow** *Erwin de Kock, Jos Verhaegh and Serge Amougou* **Session 8B: Synthesis of Executable Extra-Functional System-Level Models for Timing and Power Exploration** *Session chair: Kim Grüttner* **8B.1 A MDD Methodology for Specification of Embedded Systems and Automatic Generation of Fast Configurable and Executable Performance Models** *Eugenio Villar, Fernando Herrera Casanueva and Francisco Ferrero Mateos* **8B.2 Energy and timing analysis and optimization of embedded applications** *William Fornaciari and Carlo Brandolese* **8B.3 From RTL IP to functional system-level models with extra-functional properties** *Daniel Lorenz, Kim Grüttner, Nicola Bombieri, Valerio Guarnieri and Sara Bocchio* **8B.4 Run-time resource management based on design space exploration** *Chantal Couvreur, Philipp A. Hartmann, Gianluca Palermo and Fabien Colas-Bigey* **8B.5 Network-aware Design-Space Exploration of a Power-Efficient Embedded Application** *Mihai Lazarescu, Parinaz Sayyah, Davide Quaglia, Emad Ebeid and Sara Bocchio*
Industry special session: **"Low power high performance computing - How could this trend help embedded systems technology?"** *Kurt Shuler (Arteris, USA), Fabien Clermidy (CEA, France), Jochen Haerdtlein (Bosch, Germany)* **Best paper award, announcements, and closing remarks**		

WORKSHOPS, TUTORIALS, AND INDUSTRY SESSIONS

SUNDAY 7th OCTOBER: TUTORIALS

CASES	EMSOFT	CODES+ISSS
Tutorial 1: Analytical Approaches for Performance Evaluation of Networks-on-Chip *Organiser: Axel Jantsch*	**Tutorial 1: Runtime Verification of Real-time Embedded Systems** *Organiser: Borzoo Bonakdarpour*	**Tutorial 1: Coarse-Grained Reconfigurable Architectures - Compilation and Exploration** *Organiser: Tom Vander Aa*
Tutorial 2: Embedded Reconfigurable Architectures *Organiser: Stephan Wong*	**Tutorial 2: Mixed critical system design and analysis** *Organiser: Rolf Ernst*	**Tutorial 2: Soft Errors: The Hardware-Software Interface** *Organiser: Kyoungwoo Lee*

SUNDAY 7th OCTOBER: WORKSHOPS

CASA 2012: Compiler-Assisted SoC Assembly *Organiser: Aviral Shrivastava*
MeCoES: Metamodeling and Code Generation for Embedded Systems *Organisers: Wolfgang Ecker and Wolfgang Mueller*
EON 2012: Optimization of Computing at the Edge of Network *Organisers: Shahrokh Daijavad, Sumedh Sathaye and Seraphin Calo*

TUESDAY 9th OCTOBER: INDUSTRY SESSION

Session 1: Trends in Automotive Embedded Systems
Trends and new Challenges in Automotive E/E Architectures *(Dan Gunnarsson, BMW, Germany)*; **New Challenges in HW and SW Integration** *(Stefan Kuntz, Continental, Germany)*; **Virtualisation Support for an Embedded Automotive Environment** *(Glenn Farrall, Infineon Technologies, UK)*; **Software Engineering for the next-generation automotive systems** *(Akihito Iwai, Denso, Japan)*.

WEDNESDAY 10th OCTOBER: INDUSTRY SESSIONS

Session 2: Internet-of-Energy - Combining Embedded Computing and Communication for the Smart Grid
Interactions of Large Scale EV Mobility and Smart Grids - Chances and Challenges of Grid Infrastructure Simulations *(Randolf Mock, Siemens, Germany)*; **Reliable Building Energy Management in the Smart Grid** *(Moritz Neukirchner, TU Braunschweig, Germany)*; **Home Networks for the Smart Grid and Other Future Applications** *(Michael Huetwohl, Lantiq, Germany)*; **Wireless Sensor Components** *(Pascal Urard, ST Microelectronics, France)*
Session 3: Research issues in smart phones, notepads and related services *Petri Liuha (Nokia, Finland), Kari Pehkonen (Renesas Mobile, Finland), Juhani Rummukainen (ST-Ericsson, Finland) and Veli-Pekka Vatula (Intel, Finland).*

THURSDAY 11th OCTOBER: WORKSHOPS/SYMPOSIA

WESS 2012: Workshop on Embedded Systems Security *Organisers: Dimitrios Serpanos*
ESTIMedia 2012: 9th IEEE Symposium on Embedded Systems for Real-Time Multimedia *Organisers: Jian-Jia Chen and Maurizio Palesi*
MeAOW 2012: Memory Architecture and Organization Workshop *Organisers: Nikil Dutt and Jason Xue*
WESE 2012: Workshop on Embedded and Cyber-Physical Systems Education *Organisers: Jeff Jackson, Peter Marwedel, and Kenneth Ricks*
RSP 2012: IEEE International Symposium on Rapid System Prototyping *Organisers: Fabiano Hessel, Jérôme Hugues, Frédéric Rousseau*

FRIDAY 12th OCTOBER: WORKSHOPS/SYMPOSIA

RSP 2012: IEEE International Symposium on Rapid System Prototyping *Organisers: Fabiano Hessel, Jérôme Hugues, Frédéric Rousseau*
ESTIMedia 2012: 9th IEEE Symposium on Embedded Systems for Real-Time Multimedia *Organisers: Jian-Jia Chen and Maurizio Palesi*

★ = **Nominated for Best Paper award**