CASES 2011

International Conference on Compilers Architectures and Synthesis of Embedded Systems

The CASES conference provides a forum for emerging technology in embedded computing systems, with an emphasis on compilers and architectures for embedded systems. CASES is a common forum for researchers with an interest in embedded systems to reach across vertically integrated communities and to promote synergies. As evident from the past CASES meetings, several emerging applications are critically dependent on these interactions for their sustained growth and evolution. CASES 2011 is part of the 2011 Embedded Systems Week.

Program Chairs:
Prof. Rajesh Gupta (University of California, San Diego) and Prof. Vincent Mooney (Georgia Institute of Technology)

Areas of Interest
Previously unpublished papers containing significant novel ideas and technical results are solicited. Conference topics include, but are not limited to, the following areas.

- **Compilers**
  - compilation techniques and compilation flows
  - compilers for low power, performance, reliability
  - Instruction-level parallelism for VLIW, EPIC and superscalar
  - programming paradigms for multi-core systems
- **Architectures**
  - multi-core system-on-chip
  - on-chip communication architectures
  - extensible, customizable ASIPs
  - run-time and design time reconfigurable processors and on-chip architectures
  - memory architectures: memory management, smart caches and compiler controlled memories
  - novel nano-based architectures
  - 3-D architectures
- **Synthesis**
  - synthesis of hardware software systems
  - thermal and power-aware synthesis flows
  - synthesis for reliability, low power, performance
  - 3-D integration and synthesis
- **Embedded Systems**
  - specification and design
  - models of computation
  - modeling and management for power/thermal, performance and reliability
  - analysis techniques for embedded system including design space exploration, co-simulation
  - validation, verification, and debugging techniques of embedded software
  - static and dynamic timing analysis
  - domain specific embedded applications

Paper Submission
Papers should represent original work, not published or submitted for publication in other forums. A blind review process will be enforced. Authors should not reveal authorship directly or indirectly through references. Papers must be in PDF format and should not exceed 10 pages in ACM two-column format (9pt on 8.5"x11" letter size paper). For formatting instructions and templates, visit the ACM web site. Formal proceedings will be published on CD-ROM and web page forms (copyright by ACM and IEEE). Please make sure your paper prints satisfactorily on the 8.5"x11" (letter) format, this is especially important for countries where A4 paper is standard. Submissions not adhering to these guidelines may be summarily rejected at the discretion of the chair. As in the past, the Program Committee may elect to accept some papers for poster and/or short paper sessions.