2026 Embedded Systems Week

OCTOBER 4–9, 2026 | BARCELONA, SPAIN

ESWEEK PROGRAM

SPONSORING SOCIETIES:

acm CAS CEDA IEEE acm SIGBED sigda acm sigmicro

WELCOME TO ESWEEK 2026

Andy D. Pimentel
General Chair
University of Amsterdam, The Netherlands

Mohammad Abdullah Al Faruque
General Co-Chair
University of California, Irvine, USA

Francisco J. Cazorla
Conference and Local Arrangement Chair
Barcelona Supercomputing Center, Spain

Jaume Abella
Local Arrangement Co-Chair
Barcelona Supercomputing Center, Spain

Sergi Abadal
Local Arrangement Co-Chair
Universitat Politècnica de Catalunya, Spain

Welcome to ESWEEK 2026 in Barcelona!

We would like to warmly welcome you to the 22nd edition of the Embedded Systems Week (ESWEEK). ESWEEK is the premier event covering all aspects of embedded systems and software, which brings together three leading conferences (CASES, CODES, and EMSOFT), one symposium (MEMOCODE), six workshops, five special sessions, a panel, six tutorials, nine education classes, two student competitions, and a Ph.D. forum and recruiting event. As such, ESWEEK presents attendees a wide range of choices unveiling state-of-the-art embedded-systems design and hardware/software architectures.

Following the journal-integrated publication model for the three conferences (CASES, CODES, and EMSOFT), all full papers accepted in the Journal Track are published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). In addition, authors had the possibility to publish Late Breaking papers in IEEE Embedded Systems Letters, and 2-page Invited Extended Abstracts in the ESWEEK Proceedings.

The technical program on Monday, Tuesday, and Wednesday consists of 28 regular sessions and 5 special sessions from the three conferences. A strong emphasis on interaction is ensured thanks to a poster presentation for each paper, during which participants can discuss the papers with the authors; a poster session is arranged after each regular session. The program also features two student competitions — the Embedded System Software Competition on Monday and the ACM SIGBED Student Research Competition on Tuesday — as well as a panel on Wednesday afternoon and the PhD Forum and recruiting event on Wednesday.

Highlights of the ESWEEK program include four keynote talks by distinguished leaders in academia and industry. On Monday morning, Prof. Farinaz Koushanfar, Siavouche Nemati-Nasser Endowed Chair Professor at UC San Diego (USA), talks about "Agentic Design Automation for Embedded Systems: The Promise, the Peril, and the Proofs". On Tuesday morning, Prof. Edward A. Lee from UC Berkeley (USA) gives a talk on "Distributed Time-Sensitive Systems". The Tuesday program also features the IEEE CEDA Luncheon keynote, given by Dr. Hsien-Hsin Sean Lee from Intel (USA), on "The Age of AI — the Good, the Bad, and the Ugly". Finally, Dr. Orlando Moreira, Chief Computer Architect for AI Cores at Snap Inc. (The Netherlands), gives a talk on Wednesday morning on "Computing Without Looking Away: Embedded AI Architectures for Always-On Smart AR Glasses".

The Test of Time Award ceremony will take place on Tuesday morning to honor the authors of CASES, CODES, and EMSOFT papers that have demonstrated to have had a major and lasting impact on their respective research fields. Regarding the Best Paper Award ceremony, it will take place on Wednesday morning, the best papers for the three conferences being selected from candidate papers presented during Monday's and Tuesday's regular sessions.

Thursday and Friday are the days for the symposium and workshops. We are excited to host one symposium, MEMOCODE (International Symposium on Formal Methods and Models for System Design), and six workshops: SDS (Workshop on Software-Defined Systems), NIPS (Workshop on Novel Designs for RISC-V Cores and Peripheral IPs), RSP (Workshop on Rapid System Prototyping), TCRS (Workshop on Time-Centric Reactive Software), WEEPQC (Workshop on European Efforts for Post Quantum Cryptography Migration and Standardization in Embedded Systems), and CAIESA (Workshop on Challenges in AI-Based Embedded Systems Applications).

The tutorials on Sunday precede the conferences and provide an excellent opportunity to get in-depth knowledge in new trends and hot topics. There are six half-day tutorials, covering a wide scope of topics: discrete abstractions for cyber-physical systems; hardware/software co-design environments for FPGA-integrated heterogeneous systems; hardware-aware compilation for analog, digital, and heterogeneous computing-in-memory systems; prototyping and validating memory solutions for multicore real-time systems; VLA-based autonomous driving; and quantum computing.

On Friday, October 2nd — the week before the on-site event — nine education classes will take place virtually, given by prominent experts in the embedded systems domain. These are excellent opportunities for students and young researchers to improve their knowledge in these topics.

We are grateful to our sponsoring societies, ACM (SIGBED, SIGDA, SIGMICRO) and IEEE (CEDA and CASS), as well as to our industrial and academic sponsors: Qualcomm (Platinum), Barcelona Supercomputing Center (Gold), and PAL Robotics (Silver). We would also like to thank IEEE CEDA for sponsoring Tuesday's lunch and the CEDA Luncheon Keynote.

The organization of ESWEEK was only possible with the continuous support and help from many volunteers: the program chairs with their program committee members, the organizers of the workshops, tutorials, education classes and symposium, all members of the organization committee, and, last but not least, the local arrangement team, including the student volunteers.

We are looking forward to meeting you in person at ESWEEK 2026 in Barcelona!

Kind Regards,
Andy D. Pimentel, General Chair
Mohammad Abdullah Al Faruque, General Co-Chair
ESWEEK 2026

ESWEEK 2026
THANK YOU TO OUR SPONSORS

PLATINUM

Qualcomm

ESWEEK 2026
THANK YOU TO OUR SPONSORS

GOLD

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

SILVER

PAL

TUESDAY'S LUNCH AND LUNCHEON KEYNOTE SPONSOR

CEDA®
IEEE Council on Electronic Design Automation

SPONSORING SOCIETIES

acm

CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY

CEDA®
IEEE Council on Electronic Design Automation

IEEE

acm SIGBED

sigda

acm sigmicro

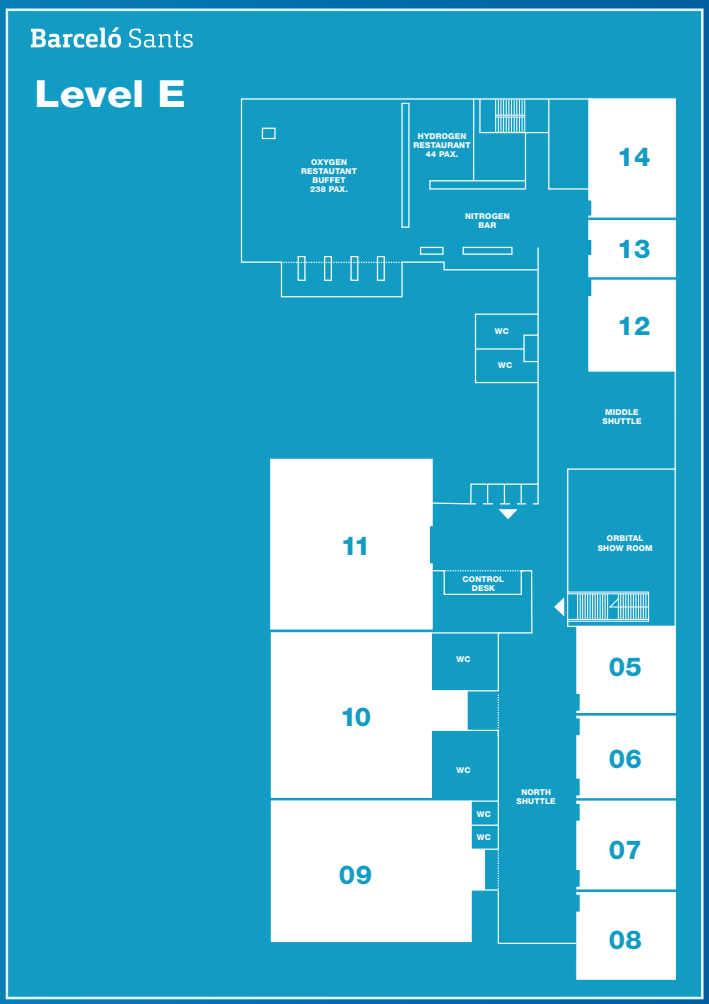
ESWEEK 2026
SCHEDULE AT-A-GLANCE

Floor Plan

Barceló Sants

Level E will be used for Sunday~Wednesday and Level 0 will be used for Thursday~Friday.

Barceló Sants



ESWEEK 2026
SCHEDULE AT-A-GLANCE

Friday, October 2 — Education Classes

	Virtual	Virtual	Virtual
8:00 - 10:00 CEST 23:00 - 1:00 MST 7:00 - 9:00 BST 9:00 - 11:00 EEST 11:30 - 13:30 IST	**Education Class 1** **Design and Analysis of Resilient Embedded Systems** Cristiana Bolchini (Politecnico di Milano)	**Education Class 2** **Architecting Domain-Tailored Computing Systems: Opportunities and Strategies** Giovanni Ansaloni (EPFL)	**Education Class 3** **System Level Data Formats and Representations for AI** Urbi Chatterjee (IIT Kanpur)
13:00 - 15:00 CEST 4:00 - 6:00 MST 12:00 - 14:00 BST 14:00 - 16:00 EEST 16:30 - 18:30 IST	**Education Class 4** **Designing Adaptive, Secure, and Sustainable Embedded Systems** Amit Kumar Singh (University of Essex)	**Education Class 5** **Lazy by Design: Bioinspired Edge AI for Efficient, High-Performance, and Robust Vision** Theocharis Theocharides (University of Cyprus)	**Education Class 6** **Reliability Challenges and Solutions for Modern AI and Emerging Accelerators** Fernando Fernandes dos Santos (Inria)
18:00 - 20:00 CEST 9:00 - 11:00 MST 17:00 - 19:00 BST 19:00 - 21:00 EEST 21:30 - 23:30 IST	**Education Class 7** **From Benchmarks to Bit-Flips: Systems View of Efficient and Reliable AI on the Edge** Gayathri Ananthanarayanan (IIT Dharwad)	**Education Class 8** **ML Compilation: Multi-Level IRs and Heterogeneous Targets** Aviral Shrivastava (Arizona State University)	**Education Class 9** **Hardware Security and Trust** Giorgio Di Natale (CNRS, TIMA)

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Sunday, October 4 — Tutorials

	ROOM: MR05	ROOM: MR06	ROOM : MR07
09:00 - 10:30	**Tutorial 1** **Accelerating Alpamayo 1 Inference via Architectural and System-Level Optimizations** Seongsoo Hong (Seoul National University), Jong-Chan Kim (Kookmin University), Namcheol Lee (Seoul National University)	**Tutorial 2** **From Application Development to Design-Space Exploration with CEDR for Heterogeneous Systems** Serhan Gener (University of Arizona) and Ali Akoglu (University of Arizona)	**Tutorial 3** **Hardware-Aware Compilation for Analog, Digital, and Heterogeneous Computing-in-Memory Systems** Jeronimo Castrillon (TU Dresden), Asif Ali Khan (TU Dresden), João Paulo Cardoso de Lima (TU Dresden)
10:30 - 11:00	**Coffee Break (North Shuttle)**		
11:00 - 12:30	**Tutorial 1** **Accelerating Alpamayo 1 Inference via Architectural and System-Level Optimizations** Seongsoo Hong (Seoul National University), Jong-Chan Kim (Kookmin University), Namcheol Lee (Seoul National University)	**Tutorial 2** **From Application Development to Design-Space Exploration with CEDR for Heterogeneous Systems** Serhan Gener (University of Arizona) and Ali Akoglu (University of Arizona)	**Tutorial 3** **Hardware-Aware Compilation for Analog, Digital, and Heterogeneous Computing-in-Memory Systems** Jeronimo Castrillon (TU Dresden), Asif Ali Khan (TU Dresden), João Paulo Cardoso de Lima (TU Dresden)
12:30 - 13:30	**Lunch Break (North Shuttle)**		
13:30 - 15:00	**Tutorial 4** **A Pragmatic Guide to Building Conservative Discrete Abstractions of Cyber-Physical Systems** Jordan Peper (University of Florida) and Ivan Ruchkin (University of Florida)	**Tutorial 5** **Large-scale simulation of Quantum circuits using Tensor Networks** Artur Garcia-Saez (Barcelona Supercomputing Center)	**Tutorial 6** **Octopus — An Open Framework for Prototyping and Validating Memory Solutions in Multicore Real-Time Systems** Mohamed Hassan (McMaster University), Yuying Lai (McMaster University), Derek Furtado (McMaster University), Guotong Miao (McMaster University)
15:00 - 15:30	**Coffee Break (North Shuttle)**		
15:30 - 17:00	**Tutorial 4** **A Pragmatic Guide to Building Conservative Discrete Abstractions of Cyber-Physical Systems** Jordan Peper (University of Florida) and Ivan Ruchkin (University of Florida)	**Tutorial 5** **Large-scale simulation of Quantum circuits using Tensor Networks** Artur Garcia-Saez (Barcelona Supercomputing Center)	**Tutorial 6** **Octopus — An Open Framework for Prototyping and Validating Memory Solutions in Multicore Real-Time Systems** Mohamed Hassan (McMaster University), Yuying Lai (McMaster University), Derek Furtado (McMaster University), Guotong Miao (McMaster University)
18:00 - 19:30	**Welcome Reception (North Shuttle)**		

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Monday, October 5 - Main Conferences, Day 1

	ROOM: MR10+11				
08:30 - 09:00	**Opening Session**				
09:00 - 10:00	**KEYNOTE 1: "Agentic Design Automation for Embedded Systems: The Promise, the Peril, and the Proofs",** Prof. Farinaz Koushanfar, UC San Diego Session Chair: Andy Pimentel				
10:00 - 10:30	**Coffee Break (North Shuttle + Orbital Shuttle)**				
	ROOM: MR05+06	**ROOM: MR07+08**	**ROOM: MR12+13**	**ROOM: MR14**	**ROOM: MR10+11 (front rows)**
10:30 - 12:00	**Session 1, CODES** **Speeding up LLMs with Sparsity, Quantization, and Speculation** Session Chair: Sudeep Pasricha	**Session 1, CASES** **Hardware Synthesis and Design Automation** Session Chair: Yu Hua	**Session 1, EMSOFT** **Edge AI and Autonomous Driving** Session Chair: Borzoo Bonakdarpour	**Session 2, CODES** **Emerging Threats and Defenses in Hardware Security** Session Chair: Umit Ogras	
10:30 - 10:45	**UnionSparse: Low-bit-width Index-Efficient Sparsity Framework for LLM Inference on edge** Tianhao Jiang, Hang Gu, Teng Wang, Qianyu Cheng, ZhenDong Zheng, Cheng Tang, Qiyue Su, Wenqi Lou, Lei Gong, Chao Wang, Xi Li, Xuehai Zhou	**SymNLO: Automated and High-Accuracy Hardware Synthesis for General Nonlinear Operators** Xiangfeng Liu, Yuan Ling, Hui Wang, Yuchen Hu, Qingnan Wu, Bingkun Yao, Xiaomeng Han, Ning Wang, Qingxu Deng, Xi Wang, Zhe Jiang, Nan Guan *Best paper candidate*	**DynaStitch: Dynamic ViT Inference via Neural Stitching for Resource-Constrained Edge Devices** Jiwon Kim, Luca Mottola, Jeho Lee, Seonghoon Park, Hojung Cha, Thiemo Voigt	**Silent Drop: Neural Network Accelerator as Covert Voltage Sensor for On-Chip Power Analysis Attacks** Huashuangyang Xu, Vincent Meyers, Mehdi Tahoori	
10:45 - 11:00	**AdaOff: An Adaptive Offloading Framework for Efficient LLM Inference on Local PCs** Zeyu Zhu, Gang Li, Peisong Wang, Zitao Mo, Jian Cheng	**LAKSA: An MLIR-based Higher-Level Synthesis Compiler for Edge Inference** Jiahong Bi, Lars Schütze, Jeronimo Castrillon	**AdROD: HyperNetwork-based Adversarially Robust Object Detection for Autonomous Driving** Yuting Wu, Dongfang Guo, Xiangzhong Luo, Qun Song, Rui Tan	**HW-BLAST: High-Throughput Power Trace Acquisition for Hardware Security Evaluation** Pablo Navarro-Torrero, Eros Camacho-Ruiz, Macarena C. Martínez-Rodríguez, Piedad Brox	
11:00 - 11:15	**SpecTwin: Accelerating Tree-based Speculative Decoding via Differential Token Quantization** Yufei Sun, Pengcheng Yao, Long Zheng, Yundong Zhang, Yu Huang, Qinggang Wang, Huize Li, Wenju Zhao, Bing Zhu, Haifeng Liu, Xiaofei Liao, Hai Jin	**GrainSim: Pre-RTL Exploration of Granularity and Tiling in Pipelined FPGA DNN Accelerators** Raehyeong Kim, Dayoung Lee, Jinyeol Kim, Seung Eun Lee	**BLADE: Lightweight Fault Resilient Semantic Segmentation on Hardware Accelerators** Jhon Ordonez, Chengmo Yang	**Active-BISA: A Lightweight Scheme for Holistic Layout Defense and Integrity Monitoring against Hardware Trojans** Prithwish Basu Roy, Mahmood Vawoo Dawood Naina, Mohammad Eslami, Samuel Pagliarini, Ozgur Sinanoglu, Ramesh Karri, Johann Knechtel	

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Monday, October 5 (continued 1 of 5)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
11:15 - 11:30	**AlloBit: Algorithm-Hardware Co-Design for Group-Wise Mixed-Bit LLM Inference on FPGA** Wenqi Lou, Hongbin Wen, Zihao Wang, Jiale Dong, Teng Wang, Lei Gong, Chao Wang, Xuehai Zhou	**AxO-ReQ: Redundancy-Aware Approximate Multipliers for Reliable Quantized Neural Acceleration** Salim Ullah, Siva Satyendra Sahoo, Akash Kumar	**RIDE: Runtime-Adaptive Inference Depth for Efficient VLA in Autonomous Driving** Haibo Hu, Lianming Huang, Qiao Li, Nan Guan, Jason Xue	**PCL-PUF: Physically Coupled Layered PUF For Machine Learning Resilience** Mohamed Alsharkawy, Hassan Nassar, Jeferson Gonzalez, Kuan-Hsun Chen, Jörg Henkel	
11:30 - 11:45	**ACAS: Adaptive Control of Inference-Time Activation Sparsity for On-Device LLMs** Ethan Lin, Youngmin Yi, Hoeseok Yang	**The Design, Integration, and Programming of an Embedded FPGA for Edge AI** Biruk Seyoum, Allen Boston, Carmine Rizzi, Kuan-Lin Chiu, Guy Eichler, Joseph Zuckerman, Lana Josipovic, Pierre-Emmanuel Gaillardon, Luca P. Carloni	**Real-Time Wafer-Level Spatial Virtual Metrology on Embedded Platforms Using Frozen Foundation Models** Hyunwoo Kim, Munyoung Lee, Seung Hyub Jeon, Kyu Sung Lee	**TDXtracted: Systematic Analysis and Exploitation of In-Band and Out-of-Band Package-Scoped Performance Telemetry in TDX** Upasana Mandal, Shubhi Shukla, Nimish Mishra, Sarani Bhattacharya, Paritosh Saxena, Debdeep Mukhopadhyay	
11:45 - 11:50	**LBR: Supernormals: Replacing Floating-Point Subnormals for Extended Range in DNN Training** Shing Wai Pun, Robert Sherrick, Steven Chin, Silviu Filip, Guy Lemieux	**Extended Abstract: Co-Design of Multiplier-Free Matrix Decompositions for TinyML CNN Implementations on FPGAs** José Juan Hernández Morales, Georgios Mentzos, Frank Hannig, Konstantinos Balaskas, Georgios Zervakis, Jörg Henkel, Jürgen Teich	**LBR: Time2Drive: Benchmarking End-to-End Autonomous Driving under Real-Time Constraints with Timed Synchronous Simulation** Hongkyun Park, Yuseong Lee, Jong-Chan Kim	**LBR: SFLGuard: Model Poisoning Mitigation in Split Federated Learning via Activation-level Attestation** Dinah Waref, Yomna Alayary, Mohamed Alsharkawy, Mohamed Aboelenien Ahmed, Hassan Nassar, Heba Khdr, Mohammed Salem, Mohamed A. Abd El Ghany, Jörg Henkel	
11:50 - 11:55	**LBR: FedEdge-LoRA: Resource-aware Low-rank Knowledge Orchestration for Federated Continual Learning on Edge** Qingshuang Sun, Zhao Yang			**Extended Abstract: Compromising HLS Watermarked Hardware IPs using HLS Trojan Attack (Extended Abstract)** Anirban Sengupta, Vishal Chourasia, Vipin Verma	
11:55 - 12:00	**LBR: PACOE: Parallel Computation and Architecture Co-exploration for LLM Inference on Parallel Systems** YongLiang Ai, Teng Wang, ZhenDong Zheng, Chao Wang, Xuehai Zhou			**Extended Abstract: HermiCache: Enclave-Aware Cache Replacement for Trusted Execution Environments** Oussama Elmnaouri, Pascal Cotret, Vianney Lapôtre, Loïc Lagadec	

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Monday, October 5 (continued 2 of 5)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
12:00 - 12:30	**Poster Session (North Shuttle)**				
12:30 - 13:30	**Lunch Break (North Shuttle + Orbital Shuttle)**				
13:30 - 15:00	**Session 3, CODES** **Emerging Accelerator Architectures and Hardware-Algorithm Co-Design** Session Chair: Christian Hakert	**Session 2, CASES** **Efficient AI Processing and Acceleration** Session Chair: Dolly Sapra	**Session 2, EMSOFT** **Formal Verification of Cyber-Physical and Hybrid Systems** Session Chair: Sara Vinco	**Session 3, CASES** **Storage and Persistent-Memory Systems** Session Chair: Hassan Nassar	**Embedded System Software Competition (ESSC)**
13:30 - 13:45	**Splitting Bottlenecks: Memory-Aware Neural Architecture Search for Multi-Branch TinyML** Chia-Yin Liu, Hashan Roshantha Mendis, Yen-Chieh Huang, Yi-Jung Chen, Pi-Cheng Hsiu *Best paper candidate*	**WinHD: Efficient Fixed-Point Model Hyperdimensional Computing for Off-the-Shelf Edge Devices** Yu-Cheng Chen, Wen Sheng Lim, Ya-Tung Tsai, Chia-Heng Tu, Yuan-Hao Chang	**Verified Numerical Semantics and Code Extraction for Simulink** Yuzhen Qi, Shuling Wang, Xiangyu Jin, Xiong Xu, Naijun Zhan	**Write Buffer Strategies for Zoned Namespace SSDs: Lessons from Hardware Verification** Lok Yin Chow, Yingjia Wang, Yuhong Liang, Ming-Chang Yang	
13:45 - 14:00	**STORM: A Sustainable Optical Systolic Array Accelerator for State-Space Models** Salma Afifi, Vigneswaran Ravindran, Ishan Thakkar, Sudeep Pasricha	**RISC-V Based Accelerator for Depthwise Separable Convolutions in Edge AI** Muhammed YILDIRIM, Özcan Öztürk	**Tolerant Barrier Certificates for Stochastic Systems** Shenghua Feng, Han Su, Hao Wu, Jie An, Mingshuai Chen, Naijun Zhan	**AggreKV: Boosting Hash-based KV-SSD Performance via Locality-Centric Optimizations** Zibin Sun, Haoyi Cui, You Zhou, Xiaogang Zhao, Fei Wu	
14:00 - 14:15	**ThAME: 3D Memory-Enabled Heterogeneous Accelerator for LLM Mixture of Experts** Pratyush Dhingra, Pramit Kumar Pal, Jana Doppa, Partha Pratim Pande *Best paper candidate*	**Design of Flexible Edge Accelerator for Mixed Dense-Sparse Spiking Neural Networks** Biao Fang, Wei Jiang, Jinyu Zhan, Wenjie Yan	**A Model Checker for Bounded Hybrid Games** Qais Hamarneh, Maike Schwammberger	**HBalloc: A High-performance Persistent Memory Allocator via Non-blocking Global Allocation and Batched Persistence** Yujie Hu, Yu Hua, Xiangyu Xiang, Aoyang Tong, Xue Liu	
14:15 - 14:30	**Uni-SFU: Algorithm-HW Co-Design for Universal SFUs via Mixed-Degree Piecewise Approximation** Miao Sun, Yucheng Huang, Mingcong Cao, Jaehyun Park, Partha Pratim Pande, Umit Ogras	**Spike-ECG: A Hardware-Aware Neuromorphic System with On-Chip Learning for Continuous Wearable ECG Monitoring** Sonam, Nitesh Narayana GS, Sujay Deb	**Synthesising State-Sensitive Safe Weakly Hard Specifications for Hybrid Dynamical Systems** Sunandan Adhikary, Akash Bhattacharya, Soumyajit Dey	**Reliving the Youth: Deterministic TRIM for Capacity-Full Parity-Based SSD RAID Arrays** Tianyu Wang, Hang Li, Chenlin Ma, Jiaxian Chen, Kecheng Huang, Minhua Lu, Rui Mao, Yi Wang *Best paper candidate*	

continues on next page

Monday, October 5 (continued 3 of 5)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
14:30 - 14:45	**APEX: Adaptive Expert Prefetching for Memory-Efficient Edge MoE Inference** Alish Kanani, Layan Badawi, Umit Ogras	**Energy-Efficient Time Series Applications on IoT Devices via Sensor-Aware Early Exit Random Forest Architectures** Sirine Belhaj, Negar Haghpanahi, Lubah Nelson, Dina Hussein, Ganapati Bhat	**5-minute presentations Extended Abstract: PAC Verification of STL for Linear Parabolic PDEs** Jiyu Zhu, Shenghua Feng, Jie An, Naijun Zhan	**Improving the Performance of Small Writes in RAID systems via Geometry-aware L2P Mapping** Zhijie Huang, Yiming Zhang, Chentao Wu, Shujie Han, Xiao Zhang, Nannan Zhao	**Embedded System Software Competition (ESSC)**
14:45 - 14:50	**LBR: MemoGuard: An Adaptive Runtime for Guarding Against Memory Traps in Communication-Limited Robot Navigation** Rajat Bhattacharjya, Hyeonjong Ju, Sing-Yao Wu, Eli Bozorgzadeh, Nikil Dutt	**LBR: LOGIQ: Log-Offset Guided Integer Quantization for Hardware-Efficient Inference** Siddharth Gupta, Yuhao Liu, Akash Kumar		**NPC: Neighbor Position Co-Aware Read Voltage Calibration for Reliable 3D NAND Flash** Junlong Zhu, Bin Gao, Beichen Ning, Xiangyu Yao, Sha Liao, Lihui Feng, Chengyun Wu, Qiao Li, Jason Xue	
14:50 - 14:55	**LBR: NTV-CIM: System-Level Assessment of Near Threshold Digital Compute-In-Memory Accelerators** Panagiotis Chaidos, Alex Maras, Georgios Alexandris, Dimitrios Soudris, Sotirios Xydis				
14:55 - 15:00	**Extended Abstract: Constrained Bayesian Optimization for DSE of Monolithic 3D DNN Accelerators with Physics-Informed Thermal Estimation** Benedikt Dietrich, Mohammed Bakr Sikal, Heba Khdr, Jörg Henkel, Iraklis Anagnostopoulos				
15:00 - 15:30	**Coffee Break & Poster Session (North Shuttle + Orbital Shuttle)**				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Monday, October 5 (continued 4 of 5)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
15:30 - 17:00	**Session 4, CODES** **Compute-in-Memory for the Edge** Session Chair: Ganapati Bhat	**Session 4, CASES** **Compilation, Optimization, and Verification** Session Chair: Preeti Ranjan Panda	**Session 3, EMSOFT** **Embedded Systems Performance, Energy, and Resource Management** Session Chair: Timothy Bourke	**Session 4, EMSOFT** **Verified Software, Model Extraction, and Formal Code Generation** Session Chair: Yasser Shoukry	**Embedded System Software Competition (ESSC)**
15:30 - 15:45	**MAC-Sort: Breaking the Memory Wall with an ACAM-Powered In-Memory Sorting Accelerator** Kun-Lin Chuang, Zhong-long You, E Ray Hsieh, Tseng-Yi Chen	**HELM: Compiler-Guided Heterogeneous Execution for Large Language Models on Memory-Constrained Systems** Atharva Khedkar, Shashwat Pandey, Aviral Shrivastava	**Lightweight Asynchronous I/O Optimization for SQLite Scan Performance on Embedded Devices** Dohwan Lee, Yewon Shin, Wook-Hee Kim, Jonghyeok Park	**SLIME: Structural Low-Level Implementation Model Extraction** Christian Hakert, Mario Guenzel, Jian-Jia Chen, Silviu Craciunas	
15:45 - 16:00	**Efficient and Variation-Tolerant Tree Inference via Compact and Scalable Mapping in Analog CAMs** Zhicheng Xu, Wenqing Shi, Pengyu Ren, Chao Li, Bo Wen, Ruibin Mao, Xunzhao Yin, Xiaobo Sharon Hu, Can Li	**MetaBOLT: Metadata-Guided Post-Link Optimization with Minimal Code Size Growth** Zichen Li, Qingyi He, Shuo Jiang, Zhanhao Liang, Chun Jason Xue, Qingan Li	**A centralized performance monitoring architecture for efficient event processing** Mohammed Sajjad Jafri, Abdur Rahman, Emon Sarkar, Mahdi Hassen, Gopishankar Thayyil, Ashwin Krishna Mani, Rodolfo Pellizzoni	**SECO: Towards Code Compaction for Simulink via Verified Equivalence Extraction** Zehong Yu, Zhuo Su, Yixiao Yang, Haowei Qiu, Rui Wang, Yu Jiang	
16:00 - 16:15	**Hardware-Algorithm Co-Design of a Reconfigurable BNN Accelerator with Ultra-Low Memory for Edge Inference** Qijin Zhu, Xiaowen Chen, Zhenyu Wu, Shiying Huang, Yu Dong, Hengzhou Yuan	**BO3: Workload-Specific Compilation Pipelines for Multi-Level Compilers** Megan Kuo, Atharva Khedkar, Aviral Shrivastava	**A Power Model of System Clocks to Minimize Energy Consumption on Constrained MCUs** Michel Rottleuthner, Thomas C. Schmidt, Matthias Wählisch	**Specification-Guided Path Shortcutting for Efficient Probabilistic Model Checking** Tsubasa Matsumoto, Kazuki Watanabe, Masaki Waga *Best paper candidate*	
16:15 - 16:30	**LoCoS: RL-based Logic and Computation Sequence Co-optimization for In-memory Computing** Jiaxing Wang, Yifan Fang, Zhipeng Lv, Dan Feng, Kang Liu	**From Scratch or from Structure? Investigating the Trade-off in Replacing Convolution** Inas Bachiri, Hamza Ouarnoughi, Arisha Al Faruque, Smail Niar, Riyadh Baghdadi	**PHiSCo: A Predictable, High-Performance, Scalable and Coherent Memory System** Mohamed Hossam, Mohamed Hassan	**Bridging SystemC and QEMU for Automated FMI/Based Virtual Platform Construction** Andrei Mihai Albu, Dario Soldi, Fabio Autieri, Enrico Macii, Sara Vinco	
16:30 - 16:45	**Utilizing Extended Register Files for Efficient GEMM on Constrained Edge Processors** Heshan Dissanayake, Darshana Jayasinghe, Liu Liu, X. Sharon Hu, Sri Parameswaran	**SDF-Edge: Synchronous Dataflow Formalism for Verifiable Neural Network Inference on Edge Devices** Mohammed Alnemari, SeokHo You, Yechan Park, HyunJin Kim, Imran Ashraf, Umar Albalawi	**Achieving Speculative Intermittent Computation on Commodity Energy Harvesting Hardware** Yida Zhang, Shao-Yu Huang, Byounguk Min, Andrew Inho Park, Gan Fang, Jongouk Choi, Changhee Jung	**Modular Extraction of Lustre Models from C Reactive Programs using Frama-C** Christophe Junke, Fabien Siron, Loïc Correnson	

Monday, October 5 (continued 5 of 5)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
16:45 - 16:50	**LBR:** **Energy Efficient Checkpointing for IMC-based AI Accelerators using 3.5D Packaging** Tanishq Kekre, Sumit K. Mandal	**LBR:** **Target-Aware Machine Outlining for Embedded RISC-V** Chen Xu, Ruozhou Xiao, Zhiwei Zhang	**LBR:** **Trend-Aware Speculative Communication for Intermittent Batteryless Systems** Jinseo Lee, Jongouk Choi, Changhee Jung, Hyunwoo Joe	**Extended Abstract:** **TASync: Time Semantics Block for Multimodal Alignment** Shaoqiu Lyu, Guangyu Wu, Hanyang Xu, Wenyong Zhang	**Embedded System Software Competition (ESSC)**
16:50 - 16:55	**LBR:** **NPEX: An NPU-PIM Design Space Explorer for Edge LLM Decoding** Jaewoo Son, Soonhoi Ha	**LBR:** **Exploiting Unused Storage Space for Ultra-Low-Power Neural Network Inference** Shiming Li, Sebastian Åkerhielm, Alessio Petruccelli, Xiaoyue Chen, Luca Mottola, Yuan Yao, Stefanos Kaxiras			
16:55 - 17:00	**Extended Abstract:** **Client Selection and Model Pruning for Energy-Efficient Federated Learning on Resource-Constrained Edge Devices** Mohamed Aboelenien Ahmed, Ayoub Ourgani, Heba Khdr, Jörg Henkel				
17:00 - 17:30	**Poster Session (North Shuttle)**				

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Tuesday, October 6 - Main Conferences, Day 2

	ROOM: MR10+11				
08:30 - 09:00	**Award Ceremony (Test of Time Awards and Society Awards)** Session Chair: Xiaobo Sharon Hu				
09:00 - 10:00	**KEYNOTE 2: "Distributed Time-Sensitive Systems", Prof. Edward Lee, UC Berkeley** Session Chair: Tei-Wei Kuo				
10:00 - 10:30	**Coffee Break (North Shuttle + Orbital Shuttle)**				
	ROOM: MR05+06	**ROOM: MR07+08**	**ROOM: MR12+13**	**ROOM: MR14**	**ROOM: MR10+11 (front rows)**
10:30 - 12:00	**Session 5, CODES** **Scalable and Resilient Storage Systems** Session Chair: Shuo-Han Chen	**Session 5, CASES** **Efficient LLM Systems and Architectures** Session Chair: Aviral Shrivastava	**Session 5, EMSOFT** **Real-Time Scheduling, Timing, and Control** Session Chair: Chengmo Yang	**Session 6, CODES** **Design and Optimization of Heterogeneous Computing Systems** Session Chair: Hashan Roshantha Mendis	**ACM SIGBED Student Research Competition (SRC)**
10:30 - 10:45	**K2O: Precise Key-to-Offset Learned Index for Read-Efficient LSM-based KV Stores** Tianren Zhou, Jinrun Yang, Zaigui Zhang, Jiaqi Luo, Qian Wei, Haijun Zhang, Xiaojun Cai, Zhaoyan Shen	**TopoCache: Data-Centric Fast Recovery and Reconfiguration for Distributed LLM Training** Xiaofei Yue, Ziming Zhao, Tingting Li, Zhaoxuan Li, Jianwei Yin	**Stability and Performance of Control Systems under Probabilistic Logical Execution Time** Yde Sinnema, Enrico Bini, Martina Maggio	**Architecting and Orchestrating Memory-Proximate SIMT Cores: A Quantitative Design Space Exploration for Processing-near-Memory in GPUs** Yusuke Kuragaki, Yuan He, Masaaki Kondo	
10:45 - 11:00	**GAS: Scaling GPU-based ANN Search to Billion-Scale through Algorithm-Storage Co-Design** Zhengrui Su, Hao Huang, Mengbai Xiao, Zhixiong Xiao, Zhaoyan Shen, Dongxiao Yu, Zhaoqi Zhou, Guoliang Li	**FIRM: Resource-Efficient Selective Error Reconstruction for Quantized LLMs** Seonha Ryu, Shinhyoung Jang, Junyoung Lee, Ilhong Suh, Yeseong Kim	**Comparing Controller Synthesis Methods with Deadline-Miss Awareness** Melanie Gallant, Marc Seide, Paolo Pazzaglia, Claudio Mandrioli, Christoph Mark, Kevin Schmidt, Frank Allgöwer, Martina Maggio	**Be NTT, Be Hash or Be Memory? A Reconfigurable Memory-Centric NTT/ Hash Accelerator for Lattice-based and Hash-based Post-quantum Cryptography** Jing Kou, Boyi Zhang, He Jiang, Liang Zhang, Yuanye Yu, Linrui Wei, Song Bian, Wang Kang	

TTA Awards

CASES 2012
SiblingRivalry: online autotuning through local competitions
Jason Ansel, Maciej Pacula, Yee Lok Wong, Cy Chan, Marek Olszewski, Una-May O'Reilly, Saman Amarasinghe

CODES 2011
PRET DRAM controller: Bank privatization for predictability and temporal isolation
Jan Reineke, Isaac Liu, Hiren D. Patel, Sungjun Kim, Edward A. Lee

EMSOFT 2011
Computing semi-algebraic invariants for polynomial dynamical systems
Jiang Liu, Naijun Zhan, and Hengjun Zhao

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Tuesday, October 6 (continued 1 of 4)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
11:00 - 11:15	**ε-STAR: An ε-relaxed Adaptive Replica Placement for Distributed File Systems in Dynamic Inter-satellite Networks** Yuqi Liu, XianZhang Chen, Yuehua Niu, Pengcheng Zhang, Run Zhang, Congming Gao	**SqzAct: Taming Activation Outliers for Efficient 4-bit LLM Inference via Block-Level Squeezing** Fangxin Liu, Xin Ju, Jingkui Yang, Zongwu Wang, Chenyang Guan, Junjie Wang, Xuanpeng Zhu, Haidong Yao, Xiankui Xiong, Wen Mei, Li Jiang, Haibing Guan	**Understanding the Pitfalls of a Differentially Private Fixed-Priority Real-Time Scheduler** Mohammad Fakhruddin Babar, Tamim Ahmed, Monowar Hasan	**TENIC: Toward Fine-Grained, Isolated, and Elastic Multi-Tenant FPGA NICs for Cloud Network Offloading** Wenbin Teng, Lei Gong, Jianfeng Bao, Teng Wang, Wenqi Lou, Chao Wang, Xuehai Zhou	
11:15 - 11:30	**Accelerating Single-Disk Failure Recovery in Erasure-Coded Storage Systems: A Load-Balanced Collaborative Repair Approach** Zhijie Huang, Haoran Li, Chentao Wu, Shujie Han, Nannan Zhao, Xiao Zhang	**Coco-Serve: A Two-Stage Framework for Model Serving on Heterogeneous Accelerators** Yaodong Zhang, Tianyu WANG, Chenlin Ma, Minhua Lu, Rui Mao, Yi Wang *Best paper candidate*	**The zeroLET Task Model and its Application to Offset Design Space Exploration** Shumo Wang, Enrico Bini, Qingxu Deng, Martina Maggio *Best paper candidate*	**Collaborative Power Optimization for Heterogeneous Edge Computing using Federated SAC** Mahmoud Tamer, Benedikt Dietrich, Heba Khdr, Mohamed A. Abd El Ghany, Jörg Henkel	
11:30 - 11:45	**CRAW: Circular Replication with Apportioned Writes for Distributed Key-value Stores** Mengying Zhao, Ying Li, Sen Zhang, Jianbo Lu, Xiaojun Cai, Zhenge Jia	**HYDRA: A Heterogeneous Chiplet DSE Framework for Serving Dynamic Hybrid LLM Workloads** Jiahao Lin, Alish Kanani, Sangwan Lee, Jaehyun Park, Umit Yusuf Ogras	**Switch Precision Where It Pays: An Optimal Scheduling Approach for Efficient Control** Debarpita Banerjee, Debasmita Lohar, Sumana Ghosh	**Contract-based Hierarchical Design Space Exploration approach for Cyber-Physical Systems** Giuseppe Scalora, Luca Brodo, Stefan Henkler	
11:45 - 11:50	**LBR: HFLSM: A Hybrid Flattened LSM-tree for Write-Efficient Key-Value Stores** Chiang Kun-Chi, Chih-Yi Lyu, Liang-Chi Chen, Yu-Ming Chang, Chien-Chung Ho, Wei-Kun Shih		**Extended Abstract: Job-Level Delay Injection for Mitigating Schedule-Based Attacks in Real-Time Systems** Arkaprava Sain, Sunandan Adhikary, Soumyajit Dey	**PIDA: Physics-Informed Design Automation with a Novel Digital Twin** Yipei Liu, Hanhan Wu, Junhuan Yang, Yuhong Song, Youzuo Lin, Weiwen Jiang, Lei Yang	
11:50 - 11:55	**LBR: Hardware-Enabled In-Place Index Maintenance for Near-Storage Streaming Vector Search** Qianyu Cheng, Yuan Sun, Chao Shi, Teng Wang, Chao Wang, Huapin Chen, Xuehai Zhou				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Tuesday, October 6 (continued 2 of 4)

11:55 - 12:00	**LBR: Thermal-Aware Write Management on 3D NAND Flash Solid State Drives** Che-Wei Chang, Cheng-En Wu				
12:00 - 12:30	**Poster Session (North Shuttle)**				
12:30 - 13:15	**Lunch Break (North Shuttle + Orbital Shuttle)**				
	ROOM: MR10+11				
13:15 - 14:00	**IEEE CEDA LUNCHEON KEYNOTE: "The Age of AI — the Good, the Bad, and the Ugly",** Dr. Hsien-Hsin Sean Lee, Intel Session Chair: Jörg Henkel				
	ROOM: MR05+06	**ROOM: MR07+08**	**ROOM: MR12+13**	**ROOM: MR14**	**ROOM: MR10+11 (front rows)**
14:00 - 15:30	**Session 7, CODES** **Design Automation and Hardware Design with AIs** Session Chair: Hassan Nassar	**Session 6, CASES** **Data-Centric and Near-Memory Architectures** Session Chair: Heba Khdr	**Session 6, EMSOFT** **Efficient AI Scheduling, Acceleration, and Hardware/Algorithm Co-Design** Session Chair: Aviral Shrivastava	**Session 7, EMSOFT** **Security, Resilience, and Robustness of CPS** Session Chair: Martina Maggio	
14:00 - 14:15	**One-Shot Cosimulation-Free Buffer Sizing for Large-Scale HLS Dataflow Designs** Roberto Bosio, Paolo Pasini, Mario Casu, Mihai Lazarescu, Luciano Lavagno *Best paper candidate*	**GraphISC: Enabling Out-of-Core Graph Processing with Distributed Computational Storage** Ssu-Hao Tsai, Wen Sheng Lim, Liang-Chi Chen, Tei-Wei Kuo, Yuan-Hao Chang	**On the Utility of Exploiting Hidden Knowledge of Third-Party Classifiers for Faster Classification** Tarek Abdelzaher, Sanjoy Baruah, Alan Burns, Alan Burns, Yigong Hu	**ENOLA: Linear-Space and Low-Overhead Control-Flow Attestation for Microcontroller-based Systems** MD Armanuzzaman, Engin Kirda, Ziming Zhao	
14:15 - 14:30	**A Novel HLS Representation for Design Space Exploration Using Multimodal Learning and Expert-Guided Methods** Chao Shi, Teng Wang, Jing Wu, Qianyu Cheng, Qinggang Zhu, Longshan Shang, Wenqi Lou, Lei Gong, Chao Wang, Xuehai Zhou	**Look Once, Compute Less: A Spatio-Temporal Redundancy-Aware CIM Accelerator for Adaptive BEV Representation** Haomin Li, Fangxin Liu, Zongwu Wang, Ning Yang, Shiyuan Huang, Yilong Zhao, Chenyang Guan, Jian Liu, Xinran Liang, Li Jiang, Haibing Guan	**Multicore+GPU Scheduling and Job-Level Batching for Real-Time Spectrum Sensing** Joseph Goh, Syed Ali, Nicholas Carter, Sarah Crowder, Samarjit Chakraborty, Bryan C. Ward, James Anderson	**VERA: A Formal Framework for Firmware-First RAS Verification** Yeqian Yang, Hongjun Dai, Jiageng Yu	
14:30 - 14:45	**ARSP: Automated Repair of Verilog Design via Semantic Partitioning** Bingkun Yao, Ning Wang, Yuchen Hu, Xiangfeng liu, Yuxin Du, Hong Gao, Zhe Jiang, Nan Guan	**SNAP: A Scalable Near-Memory Accelerator for High-Throughput Private Information Retrieval** Chenzheng Jia, Zehao Chen, Zimeng Zhou, Shiqing Li, Lei Ju	**ORBIT: Operator-driven Reasoning for Branching ISA Extension Design in Edge AI** Yaqi Han, Jingzhuo Yuan, Zhijie Yang, Renzhi Chen, Naitian Zhang, Rui Gong, Li Shen, Lei Wang	**Interval POMDP Shielding for Imperfect-Perception Agents** William Scarbro, Ravi Mangal *Best paper candidate*	

continues on next page

Tuesday, October 6 (continued 3 of 4)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
14:45 - 15:00	**RTLGuard: Intent-Driven RTL Vulnerability Detection via LLMs** Hao Shen, Mingsong Chen	**QCFlash: Bulk Bitwise Processing in 3D NAND with Dynamic Sensing and Quad-level Encoding** Habib Ur Rahman, Tharini Suresh, Aleksandar Milenkovic, Sudeep Pasricha, Biswajit Ray	**PACE: Deployment-Time Scheduling Policy for Deadline-Aware, Adaptive Intermittent Inference** Pouya Mahdi Gholami, Mingyuan Xiang, Henry Hoffmann	**Spatial Resiliency in Cyber-Physical Systems** Zeyu Zhang, Hongkai Chen, Nicola Paoletti, Shan Lin, Scott Smolka	
15:00 - 15:15	**SpiceDiff-Agent: Simulation-Efficient LLM-Guided Planning for Specification-Driven Analog Circuit Netlist Repair** Zhe Feng, Yutong Ye, Jianxun Zhou, Wenbin Guo, Lihua Xu, Wendong Lu, Yunlai Zhu, Zuyu Xu, Zuheng Wu, Yuehua Dai	**ADEPT: Architecture-Driven Energy-Efficient CNN Fine-Tuning on PIM Accelerators** Pratyush Dhingra, Vibhanshu Sharma, Jana Doppa, Partha Pratim Pande	**Branch and Bound for Relational Verification of Neural Networks** Kota Fukuda, Zhenya Zhang, Guanqin Zhang, Jianjun Zhao	**Diffusion-Guided Search via Exponential Tilting (DiffTilt): An Application to Falsification of Safety-Critical Systems** Tanmay Khandait, Preetom Biswas, Hideki Okamoto, Bardh Hoxha, Georgios Fainekos, Giulia Pedrielli	
15:15 - 15:20	**LBR: UnStrip: Unlocking Structurally Robust Stripped Functionality Logic Locking with ROBDD** Praveen Karmakar, Mukesh Barpete, Chandan Karfa, Sukanta Bhattacharjee	**HIRMA: A System-Level Multi-bit RRAM Architecture for Embedded HSI Transformers** Tze-Rong Jian, Shuo-Han Chen, E Ray Hsieh, Tseng-Yi Chen	**Extended Abstract: Bootstrapped RL for Safety-driven Scheduling of Edge-Cloud Partitioned Perception DNNs in CPS** Prateek Ganguli, Tingan Zhu, Hashan Roshantha Mendis, Pi-Cheng Hsiu, Parasara Sridhar Duggirala, Samarjit Chakraborty	**LBR: FedSRAM-PUF: Federated Bit-Error Correction for Reliable SRAM PUF Authentication** Chandranshu Gupta, Meghna Kapoor, Gaurav Varshney	
15:20 - 15:25	**LBR: NeuSym-HLS: Efficient Hardware Acceleration of Deep Neural Networks with Symbolic Distillation and High-level Synthesis** Chung-Mou Pan, Swarnalata Panigrahy, Salma Elmalaki, Yasser Shoukry, Sitao Huang			**LBR: An Orchestrated Sandbox for Side-Channel Analysis of Cyber-Physical Systems Malware** Meet Udeshi, Venkata Sai Charan Putrevu, Prashanth Krishnamurthy, Ramesh Karri, Farshad Khorrami	
15:25 - 15:30					
15:30 - 16:00	**Coffee Break & Poster Session (North Shuttle + Orbital Shuttle)**				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Tuesday, October 6 (continued 4 of 4)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
	A Special Afternoon of Discovery: Special Sessions				
16:00 - 17:30	**Special Session 1, CODES** **Chiplets at Scale: Overcoming Design, Security, Photonic and Thermal Challenges for Next-Generation Heterogeneous Systems** Organizers: Sudeep Pasricha and Amit Kumar Singh	**Special Session 2, CASES** **A Cross-Stack Approach to Efficient and Scalable Generative AI** Organizers: Partha Pratim Pande, Jeronimo Castrilon Mazo, Priyadarshini Panda, and Shubham Rai	**Special Session 3, EMSOFT** **Making Time-Sensitive Networking Deployable: A Comprehensive Lifecycle Architecture** Organizer: Sebastian Steinhorst	**Special Session 4, CODES** **Neuromorphic and Analog Computing for AI-Driven Autonomous Laboratories and Robotics** Organizers: Anup Das and Antonino Tumeo	**Special Session 5, CASES** **Hardware-Software Co-Design of Quantum Machine Learning Systems** Organizers: Muhammad Kashif, Alberto Marchisio, Nouhaila Innan, and Muhammad Shafique
	Pressing Design Challenges for Multi-Chiplet Systems Amit Kumar Singh, University of Essex **Hardware Trojan Threats to Multi-Chiplet Photonic Neural Network Accelerators** Sudeep Pasricha, Colorado State University **Thermally-reliable and High-Performance Silicon Photonics Network-on-Interposer for LLM Inference** Krishnendu Chakrabarty, Arizona State University **High-Performance and Thermally Feasible Heterogeneous Multi-Chiplet Architectures** Partha Pratim Pande, Washington State University	**Co-Design of Heterogeneous 2.5D/3D Systems for Billion Parameter Generative AI Models** Partha Pratim Pande, Washington State University **Compilers for In-Memory Computing Systems** Jeronimo Castrillon Mazo, TU Dresden **Cross-layer Techniques for Efficient and Scalable LLM Deployment** Priya Panda, University of Southern California **Token Merging and Clustering** Shubham Rai, Robert Bosch Corporate Research	**From TSN Mechanisms to Deployable Networks: Joint Configuration Across Shapers and Domains** Paul Pop, Technical University of Denmark **From Standards to Systems: What the TSN Ecosystem Still Owes Industry** Silviu S. Craciunas, NXP Semiconductors and Technical University of Denmark **Windows Precedence Exclusion (WPEx): A Method to Reconfigure the TSN Time Aware Shaper without Reconfiguring the Gate Schedule** Marc Boyer, ONERA **Large Language Models for TSN Management and Orchestration: From Integration to Benchmarking** Rubi Debnath, Technical University of Munich **Panel with presenters** Moderator: Sebastian Steinhorst, Technical University of Munich	**Reconfigurable Mixed-Signal Embedded FPAA ICs** Jennifer Hasler, Georgia Tech **Autoregressive Associative Memory Decoding on Analog Crossbar** Anup Das, Drexel University **Neuromorphic and Analog Computing for Autonomous Scientific Workflows** Antonino Tumeo, PNNL **Panel and Q/A with all the speakers**	**Recursive Self-Programming Quantum Learning: A Closed- Loop Framework for Design, Compilation, and Evaluation** Samuel Yen-Chi Chen, Wells Fargo, New York **Limitations and Opportunities with Quantum Machine Learning: Experimental Studies** Anupam Chattopadhyay, Nanyang Technological University **Bridging Hardware and Software: Optimizing Quantum Compilation and Benchmarking for Scalable Quantum System** Sebastian Feld, Delft University of Technology **Co-Design Frameworks for Hybrid Quantum Neural Networks** Muhammad Shafique, New York University (NYU) Abu Dhabi
19:30 - 23:00	**Banquet — Drassanes Reials de Barcelona (Royal Shipyards of Barcelona)**				

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Wednesday, October 7 - Main Conferences, Day 3

	ROOM: MR10+11				
08:30 - 09:00	**Award Ceremony (Best Paper Awards, Competition Awards, and Society Awards)** Session Chair: Xiaobo Sharon Hu				
09:00 - 10:00	**KEYNOTE 3: "Computing Without Looking Away: Embedded AI Architectures for Always-On Smart AR Glasses", Dr. Orlando Moreira, Snap Inc.** Session Chair: Mohammad Al Faruque				
10:00 - 10:30	**Coffee Break (North Shuttle + Orbital Shuttle)**				
	ROOM: MR05+06	**ROOM: MR07+08**	**ROOM: MR12+13**	**ROOM: MR14**	**ROOM: MR10+11 (front rows)**
10:30 - 12:00	**Session 8, CODES** **Efficient and Adaptive Edge Sensing Systems** Session Chair: Oliver Bringmann	**Session 7, CASES** **Security, Cryptography, and Resilience** Session Chair: Leonidas Kosmidis	**Session 8, EMSOFT** **Distributed, Networked, and Coordinated Cyber-Physical Systems** Session Chair: Salma Elmaleki	**Session 9, EMSOFT** **Embedded Software, Storage, OS, and Verified Low-Level Implementation** Session Chair: Li-Pin Chang	
10:30 - 10:45	**BHAR: A System-Level Optimization Framework for Multisensor Batteryless Human Activity Recognition** Geffen Cooper, Nathan Tsao, Filippos Fotiadis, Ufuk Topcu, Radu Marculescu	**Replacing Explicit Error Generation With Approximate Computing in LWE-Based Schemes** Diamante Simone Crescenzo, Emanuele Valea, Alberto Bosio	**Learning-Guided Integrated Scheduling for ATS-Enabled Time-Sensitive Networking** Cheng Long, Zonghui Li, Yu Huang, Jiamin Cui	**SqueezeDisk: Bridging High-Ratio Compression and Low-Amplification Decompression in Block Storage** Zhihao Zhang, Qiao Li, Shiyu Wang, Huiba Li, Jiwu Shu, Kai Chen, Yiming Zhang	
10:45 - 11:00	**CoInfer: Sensor-to-Device Co-Inference for Embedded Vision-Language Models with Question-Aware On-Sensor Grounding** Seongjin Yun, GeonJu Park, Seungtae Hong, Youjin Kim, Jeong-Si Kim	**An Efficient and Universal Decoding Algorithm for Highly Fault-tolerant Erasure Codes** Zhijie Huang, Chengjia Zhao, Yiwei Gan, Chentao Wu, Nannan Zhao, Xiao Zhang	**Event-Triggered Decoupled MARL for Real-Time Swarm UAV Control Under Embedded Constraints** Seungdoek Roh, Sohee Park, Daeseon Choi	**ALLI/O IDE: Portable Embedded Programming via Action-based Diagram and Automatic Code Generation** Nuntipat Narkthong, Chattriya Jariyavajee, Xiaolin Xu	
11:00 - 11:15	**Federated Indoor Localization with Progressive Adaptation and Staleness-Aware Aggregation Under Sequential Domain Shifts** Sri Lakshmi Gandraspalli Raja Reddy, Akhil Singampalli, Sudeep Pasricha	**PivotOT: Resource-Constrained Cross-Layer Security Event Alignment for Edge and Embedded Systems** Fanqi Kong, Zhipeng Liu, Ziming Zhao, Junyu Chen, Zhaoxuan Li, Tingting Li, Meng Wang, Dujuan Gu, Yu Li, Qiang Xu	**Coherence in Control: Bridging Many-Core Mapping and Routing through Cost Unification** Guochu Xiong, Xiangzhong Luo, Weichen Liu	**Correct-by-construction code generation for Human-Machine Interfaces on heterogeneous safety-critical systems** Charlie Grand, Thomas Carle, Mathias Paulin, Philippe Vergnaud	
11:15 - 11:30	**TAPAS: Throughput-adaptive Perception for Autonomous Systems** Aman Vyas, Vasista Kodumagulla, Zain Taufique, Pasi Liljeberg, Anil Kanduri	**Accel-Spectre: Accelerating Spectre Attacks to Leak Run-time data** Sibani Sasmala, Keshav Goel, Sujay Deb	**Suborbital and Orbital Real-Time Localization of Gamma-Ray Bursts via Utility-Guided Coordination** Daisy Wang, Ye Htet, Jeremy Buhler, Filip Markovic, Marion Sudvarg	**Beyond the Monolithic Scheduler: Lightweight Adaptive Policy Switcher for Process Scheduling Optimization** Xinbo Wang, Shian Jia, Ziyang Huang, Jing Cao, Mingli Song	

continues on next page

Wednesday, October 7 (continued 1 of 4)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
11:30 - 11:45	**Biosense: A Multimodal IoT-Enabled Platform Integrating Surface Plasmon Resonance and Electrochemical Impedance Spectroscopy for Decentralized Diagnostics** Anderson Manoel de Azevedo Pereira, Arthur Aprígio de Melo, Gutemberg Gonçalves dos Santos Júnior, Antonio Marcus Nogueira Lima	**AEAx: Authenticated Encryption for Resource-Constrained Devices using Approximation in ARX-Transformation** Vivekananda G, Thejaswini P, Sumit K. Mandal, John Jose, Sukumar Nandi	**Expenditure-Optimal Charging for Fixed-Route Electric Vehicles Under Bounded Tardiness** Dipankar Mandal, Arshdeep Singh, Arnab Sarkar, Arijit Mondal	**Improving Aligned Memory Copies of CompCert** Alexandre Bérard, Benjamin Bonneau, Sylvain Boulmé, David Monniaux	
11:45 - 11:50	**LBR: Why Are Differentiable Weightless Neural Networks Robust to Sensor Noise? : Three Mechanisms for Edge HAR** Chaebin Lee, Jihyeon Hwang, Taehong Min, Seung Eun Lee	**LBR: WAX: Metric-Hardness-Based Lightweight Block Cipher for Post-Quantum IoT Security on 32-bit Microcontrollers** FURSAN THABIT, M. Y. Abd-Rabbou, Ibtisam Ehsan, Wadha Al-Khater, Shangru Zhao, Yuqing Zhang	**LBR: ESOC: An Attack-aware Schedule Optimisation Strategy for CAN-based systems** Sunandan Adhikary, Ipsita Koley, Shuvam Saha, Soumyadeep Das, Soumyajit Dey	**LBR: SIMD-Accelerated Parity Game Solving for Formal Verification via Strahler Progress Measures** Vanessa Flügel, Marcin Jurdzinski, Guillermo A. Perez	
11:50 - 11:55	**LBR: MeanField Surrogate Modeling for Scalable Runtime Scheduling of Concurrent Heterogeneous AI Inference on Shared GPUs** Youssef Ennouri, Soonhoi Ha				
11:55 - 12:00	**Extended Abstract: CEDR 2.0: A Lightweight Runtime Architecture for Dynamic Heterogeneous Systems** Sahil Hassan, Serhan Gener, Mustafa Ghanim, Joshua Mack, Kutalp Dilber, Aditya Ukarande, H. Umut Suluhan, Shilpa Mysore Srinivasa Murthy, Jacob Holtom, Daniel W. Bliss, Chaitali Chakrabarti, Umit Ogras				
12:00 - 12:30	**Poster Session (North Shuttle)**				
12:30 - 13:30	**Lunch Break (North Shuttle + Orbital Shuttle)**				

continues on next page

Wednesday, October 7 (continued 2 of 4)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
13:30 - 15:00	**Session 9, CODES** **Efficient and Robust AI Systems and Architectures** Session Chair: Tseng-Yi Chen	**Session 8, CASES** **Emerging and Specialized Architectures** Session Chair: Ganapati Bhat	**Session 10, EMSOFT** **Timing Semantics, Runtime Monitoring, and Specification Analysis** Session Chair: Twan Basten	**Session 9, CASES** **Adaptive Computing and System Optimization** Session Chair: Amit K Singh	**PhD Forum and Recruitment Event**
13:30 - 13:45	**GRAB: Accelerating Batched Graph-Based Retrieval on 3D-Stacked PIM Architecture** Zhaoyu Zhong, Tianyu Wang, Chenlin Ma, Jiaxian Chen, Kecheng Huang, Minhua Lu, Rui Mao, Yi Wang	**ReQuan: A Reconfigurable Low-Power Cryogenic-Aware Ising Hardware Architecture for Fast 2D/3D Surface-Code Quantum Error Correction** Haoyuan Li, Zhenzhe Chen, Quan Cheng, Kexin Shi, Weirong Dong, Feng Liang, Takashi Sato	**JSEC: Jitter-to-Step Execution Contracts for Reproducible Distributed ECU-in-the-Loop Co-Simulation** Hyunjung Lee, Daejin Park	**An end-to-end Zeroth-Order Edge Training Framework for Ultra-Low Power RISC-V MCUs** Jan Snoeijs, Run Wang, Victor Jung, Alessio Burrello, Erfan Azarkhish, Luca Benini	
13:45 - 14:00	**Robustness-Aware On-Device Unlearning for Quantized Adversarially Trained Models** Sangmin Jeon, Eunsu Cho, Woojoo Lee	**ReVolt: Power Delivery Network-Aware Voltage Droop Control for 2.5D PIM Chiplet Architectures** Vibhanshu Sharma, Alish Kanani, Miao Sun, Jana Doppa, Umit Yusuf Ogras, Partha Pratim Pande	**FAR-STL: Filter-Aware Robust Signal Temporal Logic for Online Monitoring of Cyber-Physical Systems** Supratim Gupta, Sobhan Chatterjee, Naijun Zhan, Partha Roop	**OSCAR: Optimizing Shared CAches by Simplifying CoheRence** Priyanka Singla, Dinesh Joshi, Aritra Bagchi, Preeti Ranjan Panda	
14:00 - 14:15	**LADS: Latency-Driven Structured Pruning for CNN Deployment at Edge** Kuan Jiang, Yijie Chen, Fuyang Zhao, Jing Huang, Wanli Chang	**M3D-FLOW: A Monolithic 3D Stackable Processing-Near-DRAM Architecture for Generative Normalizing Flow Applications** Bipin Thapa Magar, Ishan Thakkar, Sudeep Pasricha	**Uniform Sampling for Timed Regular Expressions** Benoît Barbot, Ezio Bartocci, Nicolas Basset, Thao Dang, Felix Gigler, Dejan Ničković	**ToolAssist: An Edge-First Function Calling Framework for Large Language Models with Adaptive Cloud Collaboration** Varatheepan Paramanayakam, Aikaterini Maria Panteleaki, Iraklis Anagnostopoulos	
14:15 - 14:30	**Bern2Edge: An End-to-End Neurosymbolic Compiler for Efficient Edge Deployment via Bernstein Polynomial Networks** Malak Gamal El-Din, Yifan Zhang, Yasser Shoukry, Sitao Huang, Salma Elmalaki	**A 3D-Stacked 8.4 TFLOPS/4.3W Many-Core Domain-Specific Processor for AI-Native Radio Access Networks** Marco Bertuletti, Yichao Zhang, Diyou Shen, Alessandro Vanelli-Coralli, Frank K. Gürkaynak, Luca Benini	**Counterexample Classification for Signal Temporal Logic Specifications** Zhenya Zhang, Parv Kapoor, Jie An, Eunsuk Kang	**Personalized Federated Hyperdimensional Computing via Shared-Personal Prototype Memory Decomposition** Shinhyoung Jang, Seohyun Kim, Hyunsei Lee, Junyoung Lee, Seonha Ryu, Chaitali Bhattacharyya, Sehyun Park, Mohsen Imani, Yeseong Kim	

continues on next page

Wednesday, October 7 (continued 3 of 4)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
14:30 - 14:45	**Viyog: Separating Adversarial and Out-of-Distribution** Aman Singh, Abhinav Kumar, Rishab Kashyap, Soyeong Park, Ameya Gurjar, Yohan Ko, Hwisoo So, Uiwon Hwang, Kyoungwoo Lee, Aviral Shrivastava	**5-minute presentations** **LBR:** **An Almost Accurate Sum of Absolute Differences Architecture for FPGAs** Muhammad Ali, Waqar Ahmad, Fahad Bin Muslim, Anees Ullah, Ayesha Khalid **LBR:** **BRILU: BRAM-Optimised LU Decomposition with RISC-V Based Hardware Accelerator** Bindu Mekala, Sri Parameswaran, Soumya J **Extended Abstract:** **Locality-Aware FPGA Acceleration of TFHE Bootstrapping Kernels** Zahra Mojtahedin, Mohamed Alsharkawy, Rayan AbdelHady, Hassan Nassar, Jörg Henkel	**Robust Spline-based Planning for Signal Temporal Logic** Samuel Williams, Jyotirmoy Deshmukh	**5-minute presentations** **LBR:** **Transfer-Aware Kernel Placement on Modern Ryzen APUs** Yongseung Yu, Yoojin Lim, Choonghan Lee, Jinse Kwon **Extended Abstract:** **Fast Power-Down Recovery System Using Non-Volatile Memory on Zephyr RTOS** Akira Urakawa, Shunki Matsuo, Masahiro Aoyagi, Yutaka Kikuchi, Hideki Takase, Takeshi Ohkawa	**PhD Forum and Recruitment Event**
14:45 - 14:50	**LBR:** **Automating Firmware Generation from Schematics for Microcontroller based Design** Christopher Besch, Janis S. Häseker, Hassan Nassar, Norbert Tóth, Jörg Henkel		**LBR:** **Privacy-Preserving Robustness-Guided Testing** Charles Koll, Houssam Abbas, Mike Rosulek		
14:50 - 14:55	**LBR:** **Securing Vision Transformers Against Adversarial Attacks via Input Purification in Trusted Execution Environments** Heba Khdr, Yiğit Oğuz, Mohamed Aboelenien Ahmed, Jeferson González-Gómez, Jörg Henkel				

continues on next page

Wednesday, October 7 (continued 4 of 4)

	ROOM: MR05+06	ROOM: MR07+08	ROOM: MR12+13	ROOM: MR14	ROOM: MR10+11 (front rows)
14:55 - 15:00	**LBR: Distributed Reactive Processing using a RISC-V Processor** Daniel Martinez, Maryam Hemmati, Nathan Allen, Partha Roop				**PhD Forum and Recruitment Event**
15:00 - 15:30	**Coffee Break & Poster Session (North Shuttle + Orbital Shuttle)**				
	ROOM: MR10+11				
15:30 - 17:00	**PANEL: "Beyond the Prompt: Embedded Education and Research in the Age of AI"** Moderator: Andreas Gerstlauer				
17:00 - 17:30	**Closing Session**				

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Thursday, October 8 - Symposium and Workshops, Day 1

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
09:00 - 10:30	**SDS**	**NIPS**	**RSP**	**MEMOCODE**	**TCRS**
	Opening Remarks by organisers **Keynote 1: "Driving European Competitiveness: Collaboration on Software-Defined Vehicles",** Stefan Bogensberger, EC DG Connect **Keynote 2: "Using Virtualization of pre-defined System-Level solutions for boosting Time to Market",** Matthias Weiss, Director R&D, NXP Semiconductors Germany GmbH **Invited talk: "Towards Trustworthy SDVs: Matching Middleware Abstractions to Hardware Resources for Non-Functional Assurance",** Enrico Mezetti, BSC **Project lightning talks: "Shift2SDV: The Shift to Software",** Michael Karner **"HAL4SDV: Hardware Abstraction Layer for a European Software Defined Vehicle Approach",** Andreas Eckel **"Code4EV: Collaborative Development Framework for Electric Software-defined Vehicles",** Eric Armengaud **"UP2DATE4SDV: Safe & Secure Modular Updates, Upgrades and Dynamic Task Reallocation for SDVs",** Gregor Nitsche	**Opening Remarks by Jaume Abella (BSC)** **Keynote 1: "From the actuator to the central compute: How RISC-V supports the transition of the car",** Kajetan Nürnberger, Infineon Technologies **Keynote 2: "Innovation with RISC-V",** Quintauris	**Opening Remarks by Georgiy Krylov (University of New Brunswick) and Amer Baghdadi (IMT Atlantique/Lab-STICC)** **Keynote: "RISCV and HW implementation",** César Fuguet – TIMA lab, France and OpenHW group	**Opening Remarks by Nan Guan, City University of Hong Kong** **Keynote: "Towards Determinism in Language Models",** Partha Roop, University of Auckland	**Opening Remarks by Hokeun Kim, Arizona State University** **Keynote: "Is Time-Critical the Same as Safety-Critical? Rethinking the Distinction in an Era of AI and Increasing System Complexity",** Samarjit Chakraborty, University of North Carolina at Chapel Hill
10:30 - 11:00	**Coffee Break**				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Thursday, October 8 (continued 1 of 3)

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
11:00 - 12:30	**SDS**	**NIPS**	**RSP**	**MEMOCODE**	**TCRS**
	Tech talk 1: "Reducing Integration Debt Through a Common Reference Platform (CRIIP) for Software-Defined Systems", Mario Driussi **Tech talk 2: "Portability of SDV Applications: One App on Different Vehicle Platforms Using the HAL4SDV Abstraction Layer ",** Tomáš Mrověc **Tech talk 3: "Twin, Connect, Demonstrate: From Co-Simulation to an Integrated Software-Defined Systems Demonstrator",** Curt Hillier, Karol Kobiela, Luis Alberto Nava **Tech talk 4: "Improving continuous development efficiency along the full project lifecycle - the CODE4EV framework for Software Defined Vehicles",** Eric Armengaud **Panel discussion on Software-Defined Systems, with panelists from industry, academia, EC, project representatives;** moderators: Michael Karner and Andreas Eckel	**Session 1: RISC-V Cores and Related IPs** **Welcome** **"SafeSoC: a Safety Island for RISC-V High-Performance MPSoCs",** Sergi Alcaide, Juan Carlos Rodriguez, Marc Grau i Fornt, Ahlame el Afghani, Francisco Fuentes, Jaume Abella **"Vicuna2.0: A Flexible Platform for Design Space Exploration for Embedded Vector Processors",** Jefferson Parker Jones, Daniel Mueller-Gritschneder **"Reducing Instructions, Increasing Intelligence: Innovative Algorithms for Future Automotive Systems",** Eleni Politi, Alexandros Dimopoulos, Angelos Maroudis, George Dimitrakopoulos **"RISC-V at Fentiss",** Ana Rísquez Navarro	**Session 1: Modeling, Simulation and Validation** Session Chair: Felipe Gohring De Magalhaes **"A Rapid and Scalable SDR Prototyping Flow for Asynchronous Over-the-Air PHY Validation",** Salim Sama-Mola, Jeremy Nadal, Fatima Hamdar, Charbel Abdel Nour and Amer Baghdadi **"Modeling Tightly Coupled Accelerators in gem5",** Iago Caran Aquino, Lucas Wanner, Sandro Rigo, Tito Mario Burini and Uanderson da Conceição Silva **"Design, Implementation and Evaluation of a RISC-V IOMMU on gem5",** Dorian Sartori, César Fuguet, Sébastien Jacq, Nicolas Bouron and Frédéric Rousseau	**Session 1: Distributed and Learning-Based CPS** Session Chair: TBD **"Contract-Based Consistency and Availability Analysis for Distributed Cyber-Physical Systems"** Yifeng Xiao, Charles D. Lutz, Mauricio Castillo-Effen, Pierluigi Nuzzo **"Stabilizing the bittide by Tuning Controllers Under Topology and Latency Constraints"** Chuanshang Yin, Supratim Gupta, Sobhan Chatterjee, Nathan Allen, Partha Roop **"Explaining Counterexamples in Neural Network Verification Using Decision Trees" (WIP)** Deborshi Chakrabarti, Aarti Kumari, Sruti Goswami, Ansuman Banerjee, Swarup Kumar Mohalik, Kumar Madhukar	**Session 1: Languages, Compilation, and Runtime Foundations** Session Chair: Hoeseok Yang **"Rosetta: Compiling SysML v2 Behavior into Lingua Franca Modal Reactors",** Sebastiano Gaiardelli, Mario Libro, Pietro Turco, Enrico Fraccaroli, Michele Lora, Samarjit Chakraborty, Franco Fummi **"Macros as Abstractions: Simplifying Code Generation for Lingua Franca",** Tassilo Tanneberger, Erling R. Jellum, Jeronimo Castrillon, Edward A. Lee **"Lingua Franca on the Patmos Processor",** Ehsan Khodadad, Luca Pezzarossa, Martin Schoeberl **"Decentralized Coordination in LF: Timing Correctness and Transient Federate Support",** Chadlia Jerad, Edward A. Lee
12:30 - 13:30	**Lunch Break**				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Thursday, October 8 (continued 2 of 3)

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
13:30 - 15:00		**NIPS**	**RSP**	**MEMOCODE**	**TCRS**
		Session 2: Novel Methods Developing RISC-V **"Lessons Learned from Designing an Asynchronous RISC-V ",** Johannes Ecker, Natalie Simson, Endri Kaja, Ralf Brederlow, Wolfgang Ecker **"Performance-driven Generation of Application-specific Instruction Set Processors",** Johannes Geier, Philipp van Kempen, Conrad Foik, Daniel Mueller-Gritschneder, Ulf Schlichtmann **"Learnings from RISC-V Core and SoC Design at the Communication and Computation Level Using Timed Handshake-Based Design",** Natalie Simson, Lucas Hennig, Mohamed Badawy, Ares Tahiraga, Johannes Ecker, Wolfgang Ecker **"Enabling Scalable Edge Intelligence in RISC-V Systems: A Hardware Accelerator and Co-Designed Software Stack",** Alexandru Drimbarean, Honorius Galmeanu **"ISOLDE Open Source Infrastructure IP",** Endri Kaja, Robert Kunzelman, Paritosh Kumar Sinha, Natalie Simson, Sebastian Prebeck, Wolfgang Ecker	**Session 2: Architectures and Accelerator Integration** Session Chair: Frederic Rousseau **"Engineering Change Orders for Communicating Processes in High-Level Synthesis",** Alireza Azadi, Paul Rigge, Ethan Mahintorabi and Kenneth Kent **"Tightly Coupled Acceleration of Compute-Intensive Kernels on RISC-V via In-Pipeline and CV-X-IF Integration",** Adrien Pellé, Lucas Bellier, Théophile Deconche, Stefan Weithoffer, Ali Al Ghouwayel and Amer Baghdadi **"Integrating RISC-V with Associative Processing on FPGA",** Jonathas Silveira, Lucas Castro, Sérgio Vargas and Lucas Wanner	**Session 2: Security and Verification of Cyber-Physical Systems** Session Chair: TBD **"Detection of Loop-Induced Arithmetic Vulnerability in Solidity via Invariant-Guided Symbolic Execution",** Md Tauseef Alam, Kartik Kaushik, Raju Halder, Abyayananda Maiti, Samrat Mondal, Neeraj Singh **"Automated Extraction and Validation of RISC-V ISA Models using Binary Lifting and Processor Verification",** Dakota Cappel, Nicholas Lucindo, Alan Skrypek, Ruochen Dai, Tuba Yavuz **"LLM-Guided Interactive Verification of Synchronous Programs", (WIP)** Akshay Tukaram Rao, Klaus Schneider	**Session 2: Resilience, Reliability, and Security** Session Chair: Sebastiano Gaiardelli **"Controlled Degradation, Not Dispatch Reordering: Semantics-Preserving Overload Control in Lingua Franca",** Yutaka Matsubara, Wenhung Kevin Huang, Akihito Iwai **"Reactor-Based Modeling of Safe Interrupt-Driven Communication for Distributed Embedded Systems",** Tejeswini Jayaramareddy, Hokeun Kim, Hoeseok Yang **"Deadline-Bounded Re-execution for Soft-Error Resilience using Reactor Models and Lingua Franca",** Hwisoo So, Hokeun Kim **"RACE-MiCS: Reliability-Aware Checkpointing and Execution-Time Bounding for Embedded Mixed-Criticality Systems",** Mohammad Abbasinia, Behnaz Ranjbar, Akash Kumar **"RISC-V Microarchitectural Attacks: No Timer, No Problem?",** Mahreen Khan, Gaëtan Bois-Baumann, Maria Mushtaq, Renaud Pacalet, Ludovic Apvrille
15:00 - 15:30	**Coffee Break**				

continues on next page

Thursday, October 8 (continued 3 of 3)

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
15:30 - 17:00		**NIPS**	**RSP**	**MEMOCODE**	**TCRS**
		Session 3: System- and Integration Methods **"Making IPs Fit: Towards Behavioral Interface Specifications and Automated IP Integration",** Robert Kunzelmann, Anton Paule, Johannes Geier, Stefan Wallentowitz, Wolfgang Ecker, Ulf Schlichtmann **"System-Level Simulation and Design Space Exploration through SystemC RISC-V Virtual Platforms",** Andrei Albu **"A Parameterizable TETRISC for the RocketChip Platform",** Markus Ulbricht, Kai Arne Hannemann, Lars Luchterhandt, Wolfgang Müller, Li Lu **"Bridging the Accuracy-Speed Gap in HW/SW Co-Design with ML-Based Performance Modeling",** Fatma Jebali, Ilmo Gourdin, Daniel Xavier Martin, Caaliph Andriamisaina **Closing by Wolfgang Ecker (Infineon Technologies)**	**Session 3: Special Session on RISC-V Extensions, Platforms and Verification** Session Chair: Kenneth Kent **"Efficient RISC-V Custom Instruction for Near Memory Computing Architecture",** Maha Kooli, Thaddée Bricout, Riccardo Alidori, Felix Resch, Tadej Murovic, Pavel Zaykov, Moritz Christamentl and Radu Grosu **"Automated OS-Level Verification for RISC-V Softcores: Bridging FPGA and Linux KernelCI",** Julio Nunes Avelar, Marcio Aparecido de Godoy Junior, Ana Luiza Paro Costa, Rodolfo Azevedo and Sandro Rigo **"Design of a RISC-V Based SoC with Machine Learning Accelerator Supporting TensorFlow Lite for Microcontrollers",** Ahmet Efe Karagoz, Emir Danisman and Berna Ors	**Session 3: Energy and Performance Optimizations** Session Chair: TBD **"Hop and Skip: A Design Space Exploration Strategy for the Analysis of Energy and Throughput Tradeoffs of Dataflow Networks"** Abrarul Karim, Joachim Falk, Jürgen Teich **"Bi-Objective (Exec. Time, Energy) Minimization"** Alain Girault, Jia-Jie Wang **Interactive Discussion**	**Session 3: Distributed Timing and Communication** Session Chair: Hokeun Kim **"Replacing Quorums with Time for Fault-Tolerant Distributed Systems",** Edward A. Lee, Shulu Li **"Deterministic BLE Communication for Federated Reactors",** Sebastiano Gaiardelli, Philipp H. Kindt, Samarjit Chakraborty **"Remote Train Control over WebTransport Orchestrated by Lingua Franca",** Rajib Chandra Das, Alexander Schulz-Rosengarten, Reinhard von Hanxleden **"ECAL: An Event-Level Timing Model for Distributed Cyber-Physical Systems",** Guangyu Feng, Edward A. Lee

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Friday, October 9 - Symposium and Workshops, Day 2

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
09:00 - 10:30	**WEEPQC**	**CAIESA**	**RSP**	**MEMOCODE**	**TCRS**
	Opening Remarks by Leonidas Kosmidis and Sergi Alcaide, Barcelona Supercomputing Center (BSC) **Keynote: European PQC Strategy,** EC Project Officer, TBD	**Opening Remarks by** - Marcelo Götz, Federal University of Rio Grande do Sul, Porto Alegre - Stefan Henkler, Hamm-Lippstadt University of Applied Sciences - Marcio Kreutz, Federal University of Rio Grande do Norte, Natal - Carlos Eduardo Pereira, Federal University of Rio Grande do Sul, Porto Alegre - Achim Rettberg, Hamm-Lippstadt University of Applied Sciences - Marco A. Wehrmeister, Federal University of Technology – Paraná, Curitiba **Keynote: "Functional Safety of AI-enabled Edge Systems",** Francisco J. Cazorla Almeida and Enrico Mezzetti, Barcelona Supercomputing Center (BSC)	**Session 4: Software and Prototyping** Session Chair: Amer Baghdadi **"Model-Driven Evaluation of LSTM-Based Intrusion Detection for FDI Attacks in Avionics Flight Dynamics",** Mobin Allahdini Hasaroeiyeh, Felipe Gohring de Magalhaes and Tarek Ould-Bachir **"Lightweight Compile-Time Object Reference Tracking for Templated JIT Compilers",** Scott Young, Kenneth Kent and Marius Pirvu **(short) "Awkernel+TECS: Component Framework for Rust-based Real-time Operating Systems",** Ryo Nishimura, Nao Yoshimura, Hiroshi Oyama and Takuya Azumi	**Keynote: "A Foundation for Compositional Cyber-Physical System Design",** Inigo Incer, University of Michigan	**Session 4: AI-Enabled Time-Sensitive Systems** Session Chair: Edward A. Lee **"Timing Behavior Analysis for Time-Sensitive Distributed Human- and Agent-in-the-Loop Cyber-Physical Systems",** Deeksha Prahlad, Dongha Kim, Pawan Kumar, Daniel Fan, Hokeun Kim **"Runtime Monitoring of Observation-Delay Tolerant RL Policies Using Lingua Franca",** Balkis Oueslati, Chadlia Jerad **"Phase-Aware Memory Repartitioning for Extended-Context Edge LLM Inference",** Youngchul Yoon, Soonhoi Ha **"Time-constrained Vision Language Model Inference using Semantic Caching for Autonomous Driving",** Chanhee Lee, Manuel Branco Nardi
10:30 - 11:00	**Coffee Break**				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Friday, October 9 (continued 1 of 3)

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
11:00 - 12:30	**WEEPQC**	**CAIESA**	**RSP**	**MEMOCODE**	**TCRS**
	Session 1: PQC Transition in IoT Session Chair: Sergi Alcaide **"QUBIP: Quantum-oriented Update to Browsers and Infrastructures for the PQ Transition"** Piedad Brox **"PQC4eMRTD: Post-Quantum Cryptography for electronic Machine-Readable Travel Documents"** Antonio Escobar **Poster Session**	**Session 1: Embedded** Session Chair: Kristian Rother **"Static Pessimistic Execution-Time Estimation for CUDA Kernels on NVIDIA Ampere GPUs",** Ali Alhalabi, Stefan Henkler, Domenic Drechsel and Achim Rettberg **"A Timing Observability approach for Conventional and AI-Based Autonomous Driving Applications",** Saran Deepak Elumalai Vijaya Nirmala Devi, Niklas Rahenbrock and Gregor Nitsche **"PPO-Based PID Gain Scheduling for Hexapod-Leg Control under Varying Gravity",** Ashton Mitchell, Aditya A. Krishnan and Hokeun Kim **"Deep Learning--Based Prediction of Communication Latency and Temporal Anomalies in ROS 2 Systems",** Leticia Pinto, Marco Wehrmeister and André Lazzaretti **(short) "Evaluating Saliency Methods for Selective Tile Processing on Embedded Object Detectors",** Andreas Vasiliou and Theocharis Theocharides	**Session 5: Security, Optimizations and Estimation** Session Chair: Georgiy Krylov **(short) "Polynomial Regression-Based Anomaly Detection on ARINC 429 Using a Custom X-Plane-Derived Dataset",** Antoine Bourassa, Felipe Gohring De Magalhaes, Ahmad Shahnejat Bushehri, Rim Zrelli and Gabriela Nicolescu **(short) "A Two-Tier Embedded ML-Based Triage System for Remote Screening and Hospital Prioritization",** Deesh Patel, Natalie Debiak, Lukash Darewych, Sashwat Sridhar, Nathan Grewal, Wissam Botros, Shawki Areibi and Gary Grewal **(short) "A Scalable Data-Driven FPGA Stochastic Ising Machine for Combinatorial Optimization",** Robin Gay and Tarek Ould-Bachir **(short) "A Benchmarking Framework for Explainability in Cyber-Physical Systems",** Laleh Akbari and Rolf Drechsler **(short) "A High-Level Methodology for Cycle-Accurate Power Estimation of Embedded Processors",** Mustapha Khairan Ghliss, Yehya Nasser, Guy Gogniat and Salam Doumiati **Concluding remarks**	**Session 4: Models, Semantics, and Real-Time Correctness** Session Chair: TBD **"SICON: Optimizing Code Generation for Simulink Continuous-Time Systems"** Hao Ding, Zhuo Su, Zehong Yu, Xiaosong Zhang **"Asymmetric Timed Refinement for Correct Post-Deployment Updates in Real-Time Systems"** Luca Brodo, Giuseppe Scalora **"Behavioral Specification of Synchronous Circuits in Sequential Circuits" (WIP)** Shunji Nishimura	**Session 5: CPS Observability and Resource Management** Session Chair: Chadlia Jerad **"Determinism and Reproducibility in Resource-Constrained Cyber-Physical System Simulation Using Operational Data",** Pawan Kumar, Aditya A. Krishnan, Hokeun Kim **"A Non-Intrusive Data Age Tracer for Real-Time ROS2 Applications",** Yundo Choi, Taekyeong Lee, Hyeong Rae Cho, Kyong Hoon Kim **"Tail Service Delay Mitigation for On-Demand Execution Module Streaming in Cloud-Edge Systems",** Janghun Lee, Daejin Park **"VEDRA: Verified and Efficient Dynamic Resource Allocation for Real-Time Radio Access Network Scheduling",** Debarpita Banerjee, Sumana Ghosh, Snigdha Das, Shilpa Budhkar, Rana Pratap Sircar
12:30 - 13:30	**Lunch Break**				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Friday, October 9 (continued 2 of 3)

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
13:30 - 15:00	**WEEPQC**	**CAIESA**		**MEMOCODE**	
	Session 2: PQC Transition in Industrial and Automotive Systems Session Chair: Antonio Escobar **"Q-FENCE: Securing Tomorrow's Digital Infrastructure with Quantum-Resistant Cryptography"** Pablo Navarro **"SMARTY: Scalable and Quantum Resilient Heterogeneous Edge Computing enabling Trustworthy AI",** TBA **Poster Session**	**Session 2: Analysis** Session Chair: Ali Alhalabi **"Resource-Efficient Embedded Radar-Based Elderly-care Activity Recognition via Dual-Branch Receptive-Field Learning",** Xiangbo Kong, Akari Takebayashi, Kenshi Saho and Kazuhide Kamiya **"Multi-Resolution Semantic Region Discovery in Embedded Operating-System Repositories",** Kristian Rother **"Toward Tamper-Resistant Traffic-Sign Recognition: A Concept for Multi-Channel Redundant Sign Coding in Safety-Critical AI-Based Embedded Vehicle Systems",** Samer Telawi **(short) "Prompt-to-Drive: Closed-Loop AI-Driven Scenario Synthesis and Verifier-Sensitive Semantic Alignment for Autonomous Driving Simulation",** Narmada Ambigapathy, Fatima Idrees, John Abah, Ali Alhalabi and Achim Rettberg **(short) "Property Refinement in Computation Tree Logic",** Luca Brodo, Giuseppe Scalora and Stefan Henkler		**Session 5: Correctness Guarantees for Reactive Systems** Session Chair: TBD **"ASM-Based Behavioral Attestation: Bridging Formal Specification and Runtime Conformance Checking of Security Properties"** Bernhard Fischer, Daniel Dorfmeister, Flavio Ferraroti, Stefan Rass, René Mayrhofer **"Learning-Aided Reach-Avoid Controller Synthesis with Formal Guarantees for Stochastic Systems" (WIP)** Shibo Yan, Xia Zeng, Hengjun Zhao, Zhengfeng Yang, Zhiming Liu **"A novel formal verification approach for Hiphop.js" (WIP)** Boqing Yin, Nathan Allen, Partha Roop **Closing Remarks by Nan Guan, City University of Hong Kong**	
15:00 - 15:30	**Coffee Break**				

continues on next page

ESWEEK 2026
SCHEDULE AT-A-GLANCE

Friday, October 9 (continued 3 of 3)

	ROOM: MR01	ROOM: MR02	ROOM: MR03	ROOM: MR04.1	ROOM: MR04.2
15:30 - 17:00	**WEEPQC**	**CAIESA**			
	Session 3: PQC in HPC, Cloud Computing and Beyond Session Chair: Leonidas Kosmidis **"Efficient Homomorphic Encryption for Secure Deep Learning Inference"** Antonio Peña **Poster Session and Closing**	**Session 3: AI** Session Chair: Fatima Idrees **"Multi-Tool Selection for Robotic Systems: Comparing Semantic Retrieval and Large Language Models",** Miguel Sousa, Luis Ramos Pinto and João Carvalho **"Quantized U-Net for Low-Latency Sugar Beet Segmentation in 5G-Enabled Edge Cyber-Physical Systems",** Viktoria Sorokina, Dzmitry Yablonski and Dmitry Dementiev **"Towards Safety and Validation of Virtualized Automotive Controllers via a Modular Testbed with Supervisory Monitoring and Standards-Aligned Fault Injection",** Fatima Idrees, Naved Afridi Rashiq, Moiz Zaheer Malik, Narmada Ambigapathy and Achim Rettberg **(short) "Application and Evaluation of Machine Learning on Embedded Devices: A Case Study on Solid Waste Classification Using TinyML",** Maxwell Rodrigues da Silva, Fatima Idrees, Marcelo Götz and Achim Rettberg **Closing by organizers**			

ESWEEK 2026 CONFERENCE INFORMATION

ESWEEK Full Program

ESWEEK Website