Call for Papers

International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
October 4 – October 9, 2026, *Barcelona, Spain*

CASES is a premier forum, where researchers, developers, and practitioners exchange information on the latest advances in design, optimization, validation, and applications of embedded systems, Internet of Things (IoT), and the emergent trend of integrating Artificial Intelligence into IoT (AIoT). The conference has a long tradition of showcasing cutting-edge research in these broad areas, covering topics including, but not limited to, hardware-software co-design and co-validation, edge AI, embedded architecture, compilers for heterogeneous systems, memory/storage technology, security/reliability, energy-efficiency of embedded systems, and domain-specific hardware accelerators.

Journal Track Submissions:
Abstract Submission: March 23, 2026
Full Paper Submission: March 30, 2026
Acceptance Notification: July 17, 2026
Late Breaking Results (LBR) Submissions:
Paper Submission: June 5, 2026
Acceptance Notification: July 17, 2026
Proposals of Workshops, Tutorials, Education Classes, and Special Sessions: March 30, 2026

All submission deadlines are firm and due by midnight (AOE).

We particularly solicit original research on the following topics:

1. AI Systems and Applications of AI at Edge
- AI/ML for embedded systems, Internet of Things (IoT), and Cyber-Physical Systems (CPS)
- Artificial Intelligence of Things (AIoT)
- Architectures, accelerators, and compilers for AI/ML and neural processing
- Neuromorphic and cognitive computing
- Analytics for embedded applications
- Validation, testing, and robustness of AI components

2. Safety, Security, and Reliability for Embedded Systems
- Hardware and software security for embedded systems, IoT, and CPS
- Architectures and compilers for energy-efficiency, reliability, and aging mitigation
- Timing, predictability, and real-time analysis
- Validation, verification, testing, and debugging of embedded software
- Fault tolerance, resilience, and secure-by-design methods

3. Memory and Storage Systems
- Memory system architecture for embedded systems
- Persistent, emerging, and non-volatile memory (ReRAM, MRAM, FeRAM, DNA storage, etc.)
- Caches, scratchpads, and compiler-controlled memories
- Reconfigurable and adaptive memory systems
- Embedded storage systems

4. Accelerators, Emerging Technologies, and Applications
- Design-space exploration, synthesis, and optimization of efficient accelerators
- Domain-specific accelerators for AI training/inference, graph analytics, and scientific computing
- Hardware-software codesign and compilers for accelerators
- Biologically inspired and unconventional computing
- Heterogeneous and domain-specific SoCs
- Flexible hybrid electronics (FHE), cyber-physical applications, AR/VR
- Processing-in-memory

5. Architectures, Compilers, and System-Level Design
- Embedded/mobile processor microarchitectures, GPUs, many-core systems
- Reconfigurable computing including FPGAs, CGRAs
- High-level synthesis
- Application-specific processor and 3D-stacked architectures
- Networks-on-Chip (NoC) and on-chip communication
- Compiler support for CPUs, GPUs, reconfigurable computing, and emerging paradigms
- Compilation techniques for memory, storage, and communication optimization
- Hardware-software co-design for approximate computing

Journal-Integrated Publication Model: All Journal-track papers accepted will be published in **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)**. All late-breaking papers accepted will be published in **IEEE Embedded Systems Letters (ESL)**.

See all details at http://www.esweek.org/author-information

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www.esweek.org/cases/