EMBEDDED SYSTEMS WEEK

2025 Embedded Systems Week

SEPTEMBER 28 - OCTOBER 3, 2025 | TAIPEI, TAIWAN

ESWEEK PROGRAM

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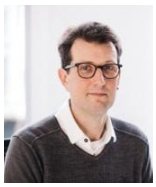
WELCOME TO ESWEEK 2025

Tei-Wei Kuo
General Chair
Delta Electronics & National Taiwan Univ, Taiwan



Andy D. Pimentel
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University of Amsterdam, The Netherlands

Yuan-Hao Chang
ESWEEK Conference Chair
National Taiwan University, Taiwan

Jen-Wei Hsieh
Local Arrangement Chair
National Taiwan Univ. of Sci. & Tech., Taiwan

Welcome to ESWEEK 2025 in Taipei!

We would like to warmly welcome you to the 21st edition of the Embedded Systems Week (ESWEEK). ESWEEK is the premier event covering all aspects of embedded systems and software, which brings together three leading conferences (CASES, CODES+ISSS, and EMSOFT), one symposium, three hot-topic workshops, five special sessions, a panel, five tutorials, five education classes, a software competition with demos, an ACM SIGBED student research competition, and a Ph.D. forum and recruiting event. As such, ESWEEK presents attendees a wide range of choices unveiling state-of-the-art embedded-systems design and hardware/software architectures.

Following the journal-integrated publication model for the three conferences (CASES, CODES+ISSS, and EMSOFT), all presented regular papers are published in the ACM Transactions on Embedded Computing Systems (TECS). In addition, authors had the possibility to publish Late Breaking papers in IEEE Embedded Systems Letters, and Work-in-Progress papers in the form of extended abstracts in the ESWEEK Proceedings.

The technical program on Monday, Tuesday, and Wednesday consists of 20 regular sessions and 5 special sessions from the three conferences. A strong emphasis on interaction is ensured thanks to a poster presentation for each paper, during which the participants can discuss the papers with the authors. In particular, a poster session is arranged after each regular session. The program also features a software competition on Monday, and a panel on "In-Memory Computing for Embedded Systems" as well as the PhD Forum and recruiting event on Wednesday.

Highlights of the ESWEEK program include four keynote talks by distinguished leaders in academia and industry. On Monday morning, Dr. Nicky Lu, Chairmain of the AI-on-Chip Taiwan Alliance (AITA) and Founder and CEO of Etron Technology (Taiwan), talks about the "Challenges in the Symbiosis between Semiconductors and AI". On Tuesday morning, Prof. David Atienza Alonso from EPFL (Switzerland) gives a talk on "Powering the Edge: AI Accelerators for Smarter and Greener Wearables". The Tuesday program also features a newly introduced CEDA Luncheon keynote given by Prof. Sanjit A. Seshia from UC Berkeley (USA). Finally, Prof. Nikil D. Dutt from the University of California, Irvine (USA) gives a talk on Wednesday morning on "Mindful AI for Adaptive, Resilient CyberPhysical Human Systems (CPHS)".

The Test of Time Award ceremony will take place on Tuesday morning to honor the authors of CASES, CODES+ISSS and EMSOFT papers published in the period of 2009 — 2011 that have demonstrated to have had a major and lasting impact on their respective research fields. Regarding the Best Paper Award ceremony, it will take place on Wednesday morning, the best papers for the three conferences being selected from candidate papers presented during Monday's and Tuesday's regular sessions.

Thursday and Friday are the days for the symposia and workshops. We are excited to host one symposium: MEMOCODE (International Symposium on Formal Methods and Models for System Design) and three workshops: MSC (Workshop on Memory and Storage Computing), RSP (Workshop on Rapid System Prototyping), and TCRS (Workshop on Time-Centric Reactive Software).

The tutorials on Sunday precede the conferences and provide an excellent opportunity to get in-depth knowledge in new trends and hot topics. There are four half-day tutorials and one full-day tutorial, covering a wide scope of topics: (1) Deep Software Stack Optimization for AI-Enabled Embedded Systems, (2) Design Automation for ML-enabled Cyber-Physical Systems, (3) Holistic Software and Hardware Design Environment for Hardware Agnostic Application Development and Deployment on FPGA-Integrated Heterogeneous Systems, (4) Approximate Arithmetic Operators for Energy-efficient AI Inference, and (5) Hardware-Aware Compilation and Simulation for In-Memory Computing.

On Friday the week before (September 26th), five education classes will take place, given by prominent experts in the embedded systems domain, and are available virtually. These are excellent opportunities for students and young researchers to improve their knowledge in these topics.

We are grateful to our ACM (SIGBED, SIGDA, SIGMICRO) and IEEE (CEDA and CASS) sponsors as well as the following industry sponsors: Delta, Lenovo, AMD, SiliconMotion, Quanta, ITRI, WNC, and Phison.

The organization of ESWEEK was only possible with the continuous support and help from many volunteers: The program chairs with their program committee members, the organizers of the workshops, tutorials, education classes and symposium, all members of the organization committee, and, last but not least, the local arrangement team, including the student volunteers.

We are looking forward to meeting you in person at ESWEEK 2025 in Taipei!

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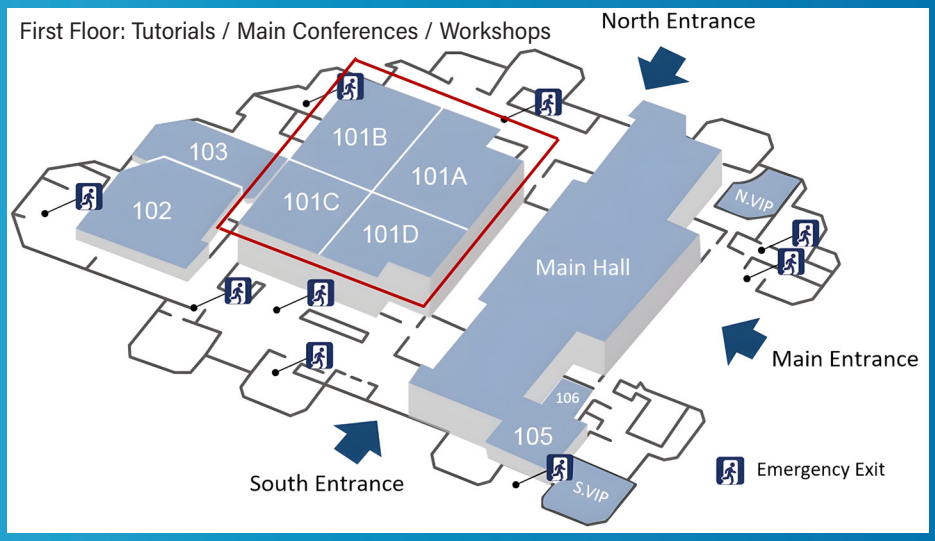
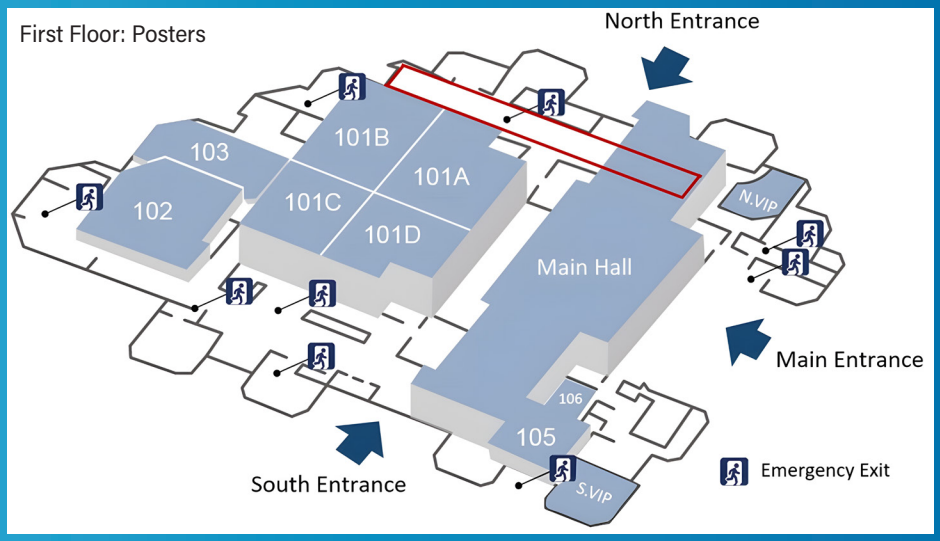
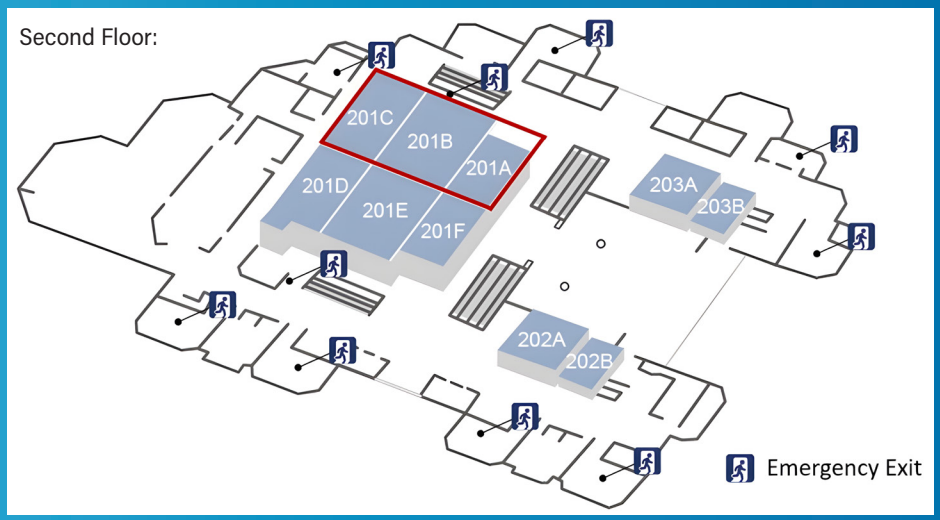
ESWEEK 2025 SCHEDULE AT-A-GLANCE

Taipei International Convention Center Floor Plan







9/29 Opening Session
9/29–10/1 Keynote 1–3
9/30 Test of Time Award Ceremony
10/1 Best Paper Award Ceremony
10/1 Panel
10/1 Closing Session

Taipei International Convention Center (TICC): No. 1, Section 5, Xinyi Road, Taipei City 110014

ESWEEK 2025 SCHEDULE AT-A-GLANCE

Friday, September 26				Classes
	Virtual	Virtual	Virtual	Virtual
08:00-10:00 (PDT, GMT-7), 11:00-13:00 (EDT, GMT-4), 17:00-19:00 (CEST, GMT+2), 23:00-01:00 (Taipei, GMT+8)	**Education Class 1** **Revisiting Approximate Computing - New Possibilities on the Horizon** Instructor: Nima TaheriNejad (Heidelberg University, Germany)	**Education Class 2** **Getting Started with the Quest RTOS and Quest-V Partitioning Hypervisor.** Instructor: Richard West, Shriram Raja, Zhiyuan Ruan (Boston University, USA), Rafiuddin Syed (Drako Motors, USA)	**Education Class 5** **Hardware-software Co-design for Printed and Flexible Electronics for Emerging On-sensor Processing Applications** Instructor: Mehdi B. Tahoori (Karlsruhe Institute of Technology, Germany)	
00:30-12:30 (PDT, GMT-7), 13:30-15:30 (EDT, GMT-4), 19:30-21:30 (CEST, GMT+2), 01:30-03:30 (Taipei, GMT+8).	**Education Class 3** **Reliability of Object Detection for Automotive and Aerospace Applications** Instructor: Paolo Rech (University of Trento, Italy)	**Education Class 4** **Neuromorphic Computing for Extremely Constrained Embedded Applications** Instructor: Stefano Di Carlo (Politecnico di Torino, Italy)		

ESWEEK 2025 SCHEDULE AT-A-GLANCE

Sunday, September 28 — Tutorials

	101A	101B	101C	101D
09:00 - 10:30	**Tutorial 1** **Deep Software Stack Optimization for AI-Enabled Embedded Systems** Author: Seongsoo Hong (SNU)	**Tutorial 2** **Design Automation for ML-enabled Cyber-Physical Systems: From Verification to Synthesis** Authors: Samarjit Chakraborty, (UNC Chapel Hill), Jingtong Hu, (University of Pittsburgh), Qi Zhu, (Northwestern University)	**Tutorial 3** **CEDR: A Holistic Software and Hardware Design Environment for Hardware Agnostic Application Development and Deployment on FPGA-Integrated Heterogeneous Systems** Authors: Serhan Gener, Sahil Hassan, Ali Akoglu (University of Arizona)	**Tutorial 4** **Design, Model, and Explore Approximate Arithmetic Operators for Energy-efficient AI Inference** Authors: Salim Ullah (Ruhr University Bochum), Siva Satyendra Sahoo (IMEC), Akash Kumar (Ruhr University Bochum)
10:30 - 11:00	**Coffee Break**			
11:00 - 12:30	**Tutorial 1** **Deep Software Stack Optimization for AI-Enabled Embedded Systems** Author: Seongsoo Hong (SNU)	**Tutorial 2** **Design Automation for ML-enabled Cyber-Physical Systems: From Verification to Synthesis** Authors: Samarjit Chakraborty, (UNC Chapel Hill), Jingtong Hu, (University of Pittsburgh), Qi Zhu, (Northwestern University)	**Tutorial 3** **CEDR: A Holistic Software and Hardware Design Environment for Hardware Agnostic Application Development and Deployment on FPGA-Integrated Heterogeneous Systems** Authors: Serhan Gener, Sahil Hassan, Ali Akoglu (University of Arizona)	**Tutorial 4** **Design, Model, and Explore Approximate Arithmetic Operators for Energy-efficient AI Inference** Authors: Salim Ullah (Ruhr University Bochum), Siva Satyendra Sahoo (IMEC), Akash Kumar (Ruhr University Bochum)
12:30 - 13:30	**Lunch Break (4F VIP Room)**			
13:30 - 15:00	**Tutorial 1** **Deep Software Stack Optimization for AI-Enabled Embedded Systems** Author: Seongsoo Hong (SNU)	**Tutorial 5** **Hardware-Aware Compilation and Simulation for In-Memory Computing** Authors: Jeronimo Castrillon, Abu Sebastian, Sharon Hu, Asif Ali Khan, Corey Lammie (Technische Universität Dresden)		
15:00 - 15:30	**Coffee Break**			
15:30 - 17:00	**Tutorial 1** **Deep Software Stack Optimization for AI-Enabled Embedded Systems** Author: Seongsoo Hong (SNU)	**Tutorial 5** **Hardware-Aware Compilation and Simulation for In-Memory Computing** Authors: Jeronimo Castrillon, Abu Sebastian, Sharon Hu, Asif Ali Khan, Corey Lammie (Technische Universität Dresden)		
18:00 - 21:30	**Reception (3F, Ballroom II, Grand Hyatt Taipei)**			

All times are Taipei Time (GMT+8)

ESWEEK 2025 SCHEDULE AT-A-GLANCE

Monday, September 29

	201ABC			
8:30 - 9:00	**Opening Session**			
9:00 - 10:00	**KEYNOTE 1: Challenges in the Symbiosis between Semiconductors and AI** Speaker: Dr. Nicky Lu, AITA — Session Chair: Tei-Wei Kuo			
10:00 - 10:30	**Coffee Break**			
	101A	**101B**	**101C**	**101D**
10:30 - 12:00	**EMSOFT 1:** **Real-Time Scheduling** Session chair: Martina Maggio	**CODES+ISSS 1:** **Mitigating Memory Bottlenecks** Session Chairs: Jason Xue and Tosiron Adegbija	**CASES 1:** **Neural Network Systems and Computing in Memory** Session Chair: Asif A. Khan	
10:30-10:50	**Transfer Schedulability in Periodic Real-Time Systems** Lars Willemsen, Mario Guenzel, Björn Brandenburg, Georg von der Brüggen, Ching-Chi Lin, Jian-Jia Chen	**System-scenario-based Design of the Last-Level Cache in Advanced Interconnect-Dominant Technology Nodes** Mahta Mayahinia, Tommaso Marinelli, Zhenlin Pei, Hsiao-Hsuan Liu, Chenyun Pan, Zsolt Tokei, Francky Catthoor, Mehdi Tahoori	**GATE: Graph Attention Neural Networks with Real-Time Edge Construction for Robust Indoor Localization using Mobile Embedded Devices.** *Best paper candidate.* Danish Gufran, Sudeep Pasricha.	
10:50-11:10	**Schedule Synthesis for Synchronous Dataflow Models with Lower and Upper Timing Bounds** Joep van Wanrooij, Twan Basten, Marc Geilen	**Re-thinking Memory-Bound Limitations in CGRAs** Xiangfeng Liu, Zhe Jiang, Anzhen Zhu, Xiaomeng Han, Mingsong Lyu, Qingxu Deng, Nan Guan *Best paper candidate*	**ERGo: Energy-Efficient Hybrid GNN Training on PIM Architectures.** Pratyush Dhingra, Chibuike E. Ugwu, Jana Doppa, Partha Pratim Pande.	
11:10-11:30	**Quasi-Static Scheduling for Deterministic Timed Concurrent Models on Multi-Core Hardware** Shaokai Lin, Erling Jellum, Mirco Theile, Tassilo Tanneberger, Binqi Sun, Chadlia Jerad, Ruomu Xu, Guangyu Feng, Magnus Mæhlum, Martin Schoeberl, Linh Thi Xuan Phan, Jeronimo Castrillon, Sanjit A. Seshia, Edward A. Lee	**SideDRAM: Integrating SoftSIMD Datapaths near DRAM Banks for Energy-Efficient Variable Precision Computation** Rafael Medina, Pengbo Yu, Alexandre Levisse, Dwaipayan Biswas, Marina Zapater, Giovanni Ansaloni, Francky Catthoor, David Atienza *Best paper candidate*	**CIMFlow: Modelling Dataflow in Cross-Layer Compute-in-Memory Deep Learning Accelerators.** José Cubero-Cascante, Lucas Tonini Rosenberg Schneider, Rebecca Pelke, Arunkumar Vaidyanathan, Rainer Leupers, Jan Moritz Joseph.	
11:30-11:50	**FC-GPU: Feedback Control GPU Scheduling for Real-time Embedded Systems** Srinivasan Subramaniyan, Xiaorui Wang *Best paper candidate*	**MERE: Hardware-Software Co-Design for Masking Cache Miss Latency in Embedded Processors** Dean You, Jieyu Jiang, Xiaoxuan Wang, Yushu Du, Zhihang Tan, Wenbo Xu, Hui Wang, Jiapeng Guan, Wang Zhenyuan, Shuai Zhao, Ran Wei, Zhe Jiang	**Luthier: Bridging Auto-Tuning and Vendor Libraries for Efficient Deep Learning Inference.** Yongin Kwon, Joohyoung Cha, Sehyeon Oh, Misun Yu, Jeman Park, Jemin Lee.	

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Monday, September 29 (continued 1 of 3)

	101A	101B	101C	101D
11:50-11:55		**Accelerating LSM-Tree KV Stores via Caching Hot Keys on Hybrid Zoned Storage** Shiqiang Nie, Menghan Li, Chi Zhang, Di Zhang, Weiguo Wu	**Work-In-Progress:** **Device Noises Resilient Training and Inference Framework for Smart Sensing on Analog Computing In Memory.** Xin-You Liu, Chi-Sheng Shih, Tsung-Te Liu, Chih-Wei Chen, Pei-Kuei Tsung, Chieh-Fang Teng.	
11:55-12:00		**RISC-V Integrated Nested Loop Analyzer for Runtime DRAM Test Pattern Generation** Saeyeon Kim, Sunyoung Park, Nahyeon Kim, Jiyoung Lee, Ji-Hoon Kim		
12:00 - 12:30	**Poster Session**			
12:30 - 13:30	**Lunch Break (4F VIP Room)**			
13:30 - 15:00	**EMSOFT 2:** **Cyber-Physical Systems** Session chair: Claudio Mandrioli	**CODES+ISSS 2:** **Reliable Neural Networks** Session Chairs: Andreas Gerstlauer and Jian Zhou	**CASES 2:** **Resource Management and Scheduling in Distributed and Heterogeneous Systems** Session Chair: Shaokai Lin	**Embedded System Software Competition**
13:30-13:50	**A Tunable Generic Meta-Heuristic Framework for Balancing Assembly Line Systems in Manufacturing** Suraj Meshram, Arnab Sarkar, Arijit Mondal	**Catch Non-determinism If You Can: Intermittent Inference of Dynamic Neural Networks** Chih-Hsuan Yen, Hashan Roshantha Mendis, Tei-Wei Kuo, Pi-Cheng Hsiu *Best paper candidate*	**Timetide: A Programming Model for Logically Synchronous Distributed Systems** Logan Kenwright, Partha Roop, Nathan Allen, Calin Cascaval, Avinash Malik. *Best paper candidate.*	
13:50-14:10	**SecureRide: Detecting Safety-threatening Behavior of E-Scooters Using Battery Information** Jiwon Kim, Geon Kim, Jeho Lee, Thiemo Voigt, Hojung Cha	**ProGIP: Protecting Gradient-based Input Perturbation Approaches for Out-of-distribution Detection From Soft Errors** Sumedh Joshi, Hwisoo So, Soyeong Park, Woobin Ko, Jinhyo Jung, Yohan Ko, Uiwon Hwang, Kyoungwoo Lee, Aviral Shrivastava	**A Load-balanced Collaborative Repair Algorithm for Single-Disk Failures in Erasure Coded Storage Systems** Zhijie Huang, Yulong Shi, Chengjia Zhao, Haoran Li, Nannan Zhao, Shujie Han, Xiao Zhang	
14:10-14:30	**Real-Time Video-based Human Action Recognition on Embedded Platforms** Ruiqi Wang, Zichen Wang, Peiqi Gao, Mingzhen Li, Jaehwan Jeong, Yihang Xu, Yejin Lee, Carolyn M. Baum, Lisa Tabor Connor, Chenyang Lu	**Lemonade: Learning-based Heterogeneous Metadata Offloading for Disaggregated Memory** Zeming Ma, Jian Zhou, Yu Fu, Xiaochang Ma, Shuhan Bai, Fei Wu	**RIMMS: Runtime Integrated Memory Management System for Heterogeneous Computing** Serhan Gener, Aditya Ukarande, Shilpa Mysore Srinivasa Murthy, Sahil Hassan, Joshua Mack, Chaitali Chakrabarti, Umit Ogras, Ali Akoglu	

Monday, September 29 (continued 2 of 3)

	101A	101B	101C	101D
14:30-14:50	**A Discrete Partial Charging enabled Dynamic Programming Strategy for Optimal Fixed-Route Electric Vehicle Charging** Dipankar Mandal, Arnab Sarkar, Arijit Mondal	**Grasp-HGN: Grasping the Unexpected** Mehrshad Zandigohar, Mallesham Dasari, Gunar Schirner	**FLIP2M: Flexible Intra-layer Parallelism and Inter-layer Pipelining for Multi-Model AR/VR workloads.** Gabriele Tombesi, Je Yang, Joseph Zuckerman, Davide Giri, William Baisi, Luca Carloni.	
14:50-14:55	**Late-Breaking: An Efficient Iterative Beam Search for Human-Robot Collaborative Assembly Line Balancing** Suraj Meshram, Sanket Jaipuriar, Arnab Sarkar, Arijit Mondal	**Detecting Non-Equivalence in Neural Networks through In-Distribution Counterexample Generation** Dina Moussa, Michael Hefenbrock, Mehdi Tahoori		
14:55-15:00		**Investigation of the Adversarial Robustness of End-to-End Deep Sensor Fusion Models** Mohamed Moslah, Ramzi Zouari, Ahmad Shahnejat, Gabriela Nicolescu, Felipe Magalhaes		
15:00 - 15:30	**Coffee Break & Poster Session**			
15:30 - 17:00	**EMSOFT 3:** **Resource Allocation** Chair: Matthias Becker	**CODES+ISSS 3:** **Synthesis and Optimizations** Session Chairs: Andy Pimentel and Gaurav Narang	**CASES 3:** **Smart Storage** Session Chair: Bryan Donyanavard	**Embedded System Software Competition**
15:30 - 15:50	**The Case for HW/SW Harmony in Real-Time Systems: Tightening Memory Latency of Streaming Applications** Abdelrhman Abotaleb, Mohamed Hassan	**FT-DAG: An Efficient Full-Topology DAG Generator with Controllable Parameters** Yinjie Fang, Liping Yang, Weichen Liu, Guoquan Zhang, Yaoyao Gu, Xiang Xiao, Wei Qin, Xiangzhen Ouyang, Wanli Chang	**Large or Small: Harnessing the Erase Duality of Emerging Bit-Alterable NAND Flash to Suppress Tail Latency** Guangliang Yao, Tsun-Yu Yang, Yingjia Wang, Tseng-Yi Chen, Ming-Chang Yang *Best paper candidate*	
15:50 - 16:10	**Towards Efficient Multi-Frame Clustering in Response Time Analysis for Large Object Communication** Jonas Peeck, Rolf Ernst, Selma Saidi *Best paper candidate*	**THERMOS: Thermally-Aware Multi-Objective Scheduling of AI Workloads on Heterogeneous Multi-Chiplet PIM Architectures** Alish Kanani, Lukas Pfromm, Harsh Sharma, Janardhan Rao Doppa, Partha Pratim Pande, Umit Ogras	**Exploiting LDPC Syndrome for Multidimensional Hard-Decoding Read Retry on NAND Flash** Szu-Wei Chen, Shuo-Han Chen	
16:10 - 16:30	**Rasco: Resource Allocation and Scheduling Co-design for DAG Applications on Multicore** Abigail Eisenklam, Robert Gifford, Georgiy A. Bondar, Yifan Cai, Tushar Sial, Linh Thi Xuan Phan, Abhishek Halder	**GNNmap: A Scalable Framework for GNN Deployment through Co-Optimized Graph Partitioning and Mapping** Zimeng Fan, Min Peng	**Page-Overwrite Data Sanitization in 3D NAND Flash: Challenges, Feasibility, and the PULSE Solution** Matchima Buddhanoy, Aleksandar Milenkovic, Sudeep Pasricha, Biswajit Ray	

Monday, September 29 (continued 3 of 3)

	101A	101B	101C	101D
16:30 - 16:50	**Late-Breaking: WCET-Aware Partitioning and Allocation of Disaggregated Networks for Multicore Systems,** Junjie Shi, Christian Hakert, Kay Heider, Mario Guenzel, Nils Hölscher, Daniel Kuhse, Jian-Jia Chen, Logan Kenwright, Sobhan Chatterjee, Nathan Allen, Partha Roop **Late-Breaking: Hybrid Software Transactional Memory for Real-Time Systems,** Zewei Chen, Maolin Yang, Yong Liao **Late-Breaking: A Configurable ReRAM Engine for Energy-Efficient Sparse Neural Network Acceleration,** I-Yang Chen, Kai-Wei Hou, Ya-Shu Chen	**FARRE: Fairness Aware Request REsponse arbitration in shared caches** Garima Modi, Priyanka Singla, Neetu Jindal, Ayan Mandal, Preeti Ranjan Panda	**ReLoaDing Performance: A Locality-Based Strategy for Rapid Reads in Encrypted Key-Value Systems.** Chi-Chieh Hung, Tseng-Yi Chen.	
16:50 - 16:55		**Work-in-Progress: CAHLS: A Source-to-Source Compiler to Generate Cycle Accurate Models for High-Level Synthesis** Yuhan She, Yanlong Huang, Jierui Liu, Ray Cheung, Hong Yan	**Late-Breaking: MdCSR: A Memory-Efficient Sparse Matrix Compression Format.** Noble G, Nalesh S, Kala S, Salim Ullah, Akash Kumar.	
16:55 - 17:00				
17:00 - 17:30	**Poster Session**			

ESWEEK 2025 SCHEDULE AT-A-GLANCE

Tuesday, September 30

	201ABC			
8:30 - 9:00	**Test of Time Award Ceremony**			
9:00 - 10:00	**KEYNOTE 2: Powering the Edge: AI Accelerators for Smarter and Greener Wearables** Speaker: Prof. David Atienza Alonso, EPFL — Session Chair: Yuan-Hao Chang			
10:00 - 10:30	**Coffee Break**			
	101A	**101B**	**101C**	**101D**
10:30 - 12:00	**EMSOFT 4:** **Hybrid and Control Systems** Session chair: Pavithra Prabhakar	**CODES+ISSS 4:** **Acceleration of AI Models** Session Chairs: Aviral Shrivastava and Madhu Mutyam	**CASES 4:** **Hardware Security and Testing** Session Chair: Amit Kumar Singh	
10:30-10:50	**Checking Bounded Reachability of Compositional Linear Hybrid Automata Using Interaction Relations** Yuhui Shi, Yuming Wu, Lei Bu, Xuandong Li	**eMamba: Efficient Acceleration Framework for Mamba Models in Edge Computing** Jiyong Kim, Jaeho Lee, Jiahao Lin, Alish Kanani, Miao Sun, Umit Ogras, Jaehyun Park	**LeakyRand: An Efficient High-fidelity Covert Channel in Fully Associative Last-level Caches with Random Eviction.** Yashika Verma, Debadatta Mishra, Mainak Chaudhuri.	
10:50-11:10	**Contract Embeddings for Layered Control Architectures** Nikhil Vijay Naik, Alessandro Pinto, Pierluigi Nuzzo	**FORT-GCN: A Fault-tolerant and Adaptive Accelerator Design for Efficient Graph Convolutional Network Inference** Ke Wang, Yingnan Zhao, Ahmed Louri	**FuSS: Coverage-Directed Hardware Fuzzing with Selective Symbolic Execution.** Aruna Jayasena, Sai Suprabhanu Nallapaneni, Prabhat Mishra.	
11:10-11:30	**A Formal Approach towards Safe and Stable Schedule Synthesis in Weakly Hard Control Systems** Debarpita Banerjee, Parasara Sridhar Duggirala, Bineet Ghosh, Sumana Ghosh	**HMSA: High-Performance Heterogeneous Mixed-Precision CNN Systolic Array Accelerator on FPGA** Yongxiang Cao, Hongxu Jiang, Huiyong Li, Yu Tang, Dongcheng Shi, Guocheng Zhao	**Robust LFSR-based Scrambling to Mitigate Stencil Attack on Main Memory.** Gaurav Kumar, Kushal Pravin Nanote, Sohan Lal, Yamuna Prasad, Satyadev Ahlawat.	

TTA Awards

Practical Aggregation of Semantical Program Properties for Machine Learning Based Optimization
Mircea Namolaru, Albert Cohen, Grigori Fursin, Ayal Zaks, and Ari Freund

Accurate Online Power Estimation and Automatic Battery Behavior Based Power Model Generation for Smartphones
Lide Zhang, Birjodh Tiwana, Robert Dick, Zhiyun Qian, Z. Morley Mao, Zhaoguang Wang, and Lei Yang

RT-Xen: Towards Real-Time Hypervisor Scheduling in Xen
Sisu Xi, Justin Wilson, Chenyang Lu, and Christopher D. Gill

continues on next page

Tuesday, September 30 (continued 1 of 3)

	101A	101B	101C	101D
11:30-11:50	**Deductive Verification of Cooperative RTOS Applications** Philip Tasche, Paula Herber, Marieke Huisman	**GINA: Exploiting Graph Neural Network Layer Features for Energy Efficient Inferencing in NVM-based PIM Accelerators** Gaurav Narang, Chukwufumnanya Ogbogu, Biresh Kumar Joardar, Janardhan Rao Doppa, Krishnendu Chakrabarty, Partha Pratim Pande	**Work-in-Progress:** **A Novel PUF Key Generation Method via Variable-Length Subkeys: An Application with Inertial MEMS Sensors.** Wacime Hadrich, Lukas Zimmermann, Axel Sikora. **Late-Breaking:** **Efficient Register-Balancing for Masked Hardware.** Nilotpola Sarma, Sujeet Narayan Kamble, Chandan Karfa.	
11:50 - 11:55	**Late-Breaking:** **Formal Modeling and Verification of Generic Credential Management Processes for Industrial Cyber-Physical Systems,** Julian Göppert, Axel Sikora	**Late-Breaking:** **QLlama: An FPGA-Based Microscaling Quantization Accelerator for Energy-Efficient Llama2 Inference** Hongbing Wen, Zihao Wang, Jiale Dong, Wenqi Lou, Lei Gong, Chao Wang, Xuehai Zhou		
11:55 - 12:00	**Work-in-Progress:** **Frequency Automata: A novel formal model of hybrid systems in combined time and frequency domains,** Moon Kim, Avinash Malik, Partha Roop	**Work-in-Progress:** **Practicalizing Tree-Based Model Acceleration with CAM through Model Pruning and Data Placement Optimization** Yi-Chun Liao, Chieh-Lin Tsai, Yuan-Hao Chang, Camélia Slimani, Jalil Boukhobza, Tei-Wei Kuo		
12:00 - 12:30	**Poster Session**			
12:30 - 13:30	**Lunch Break & CEDA Luncheon Keynote: Full-Stack AI-Enabled Formal Methods: Past, Present, and Future** Speaker: Prof. Sanjit A. Seshia, UC Berkeley — Session Chair: L. Miguel Silveira (3F, Banquet Hall)			
13:30 - 15:00	**EMSOFT 5:** **Logic and Verification** Session Chair: Timothy Bourke	**CODES+ISSS 5:** **Security Attacks and Countermeasures** Session Chairs: Sudeep Pasricha and Felipe Magalhaes	**CASES 5:** **Chiplet Architectures, Multiprocessors and Transformers Acceleration** Session Chair: Priyanka Singla	**ACM SIGBED Student Rsearch Competition**

Tuesday, September 30 (continued 2 of 3)

	101A	101B	101C	101D
13:30 - 13:50	**Efficient Black-Box Checking with Specification-Guided Abstraction** Tsubasa Matsumoto, Kazuki Watanabe, Kohei Suenaga, Masaki Waga	**DPReF: Decentralized Key Generation Using Physical-Related Functions** Mohamed Alsharkawy, Hassan Nassar, Jeferson Gonzalez-Gomez, Xun Xiao, Osama Abboud, Joerg Henkel	**On Optimizing Intra- and Inter-chiplet Interconnection Networks in Multi-chiplet Systems for Accelerating FHE Encrypted Neural Network Applications** Zewei Lai, Jinhui Ye, Xiaohang Wang, Zheang Fu, Amit Kumar Singh, Yingtao Jiang, Kui Ren, Mei Yang, Sihai Qiu, Xiaodong Li, Xin Tang, Jie Song, Mingzhe Zhang	
13:50 - 14:10	**STL-GO: Spatio-Temporal Logic with Graph Operators for Distributed Systems with Multiple Network Topologies** Yiqi Zhao, Xinyi Yu, Bardh Hoxha, Georgios Fainekos, Jyotirmoy V. Deshmukh, Lars Lindemann	**Selective Subarray Isolation for Mitigating RowHammer Attack** Praseetha M, Madhu Mutyam, Venkata Kalyan Tavva	**Designing High-performance and Thermally Feasible Multi-Chiplet Architectures Enabled by Non-bendable Glass Interposers** Harsh Sharma, Jana Doppa, Umit Yusuf Ogras, Partha Pratim Pande.	
14:10 - 14:30	**A Tree-Shaped Tableau for Checking the Satisfiability of Signal Temporal Logic with Bounded Temporal Operators** Beatrice Melani, Ezio Bartocci, Michele Chiari	**A Severe Vulnerability and an Effective Defense Against DFA on Ascon** Smita Das, Amit Jana, Debdeep Mukhopadhyay	**SHARP: SHARing-aware Cache Writeback byPass** Dinesh Joshi, Aritra Bagchi, Preeti Ranjan Panda	
14:30 - 14:50	**Cumulative-Time Signal Temporal Logic** Hongkai Chen, Zeyu Zhang, Shouvik Roy, Ezio Bartocci, Scott Smolka, Scott D. Stoller, Shan Lin *Best paper candidate*	**DynHaMo: Dynamic Hardware-based Monitoring dedicated to Attacks Detection** Juliette Pottier, Bertrand Le Gal, Maria Méndez Real, Sébastien Pillement	**Late-Breaking:** **Fused Tensor Core: A Hardware-Software Co-Design for Efficient Execution of Attentions on GPUs.** Reza Jahadi, Phil Munz, Ehsan Atoofian. **Work-in-Progress:** **I-FlashAttention: Fully Integer Fused Attention for Efficient Vision Transformers.** Sehyeon Oh, Yongin Kwon, Jemin Lee. **Work-in-Progress:** **RISC-TAE: Instruction Set Extension for Transformer Model Acceleration.** Fei Liu, Yanping Shao, Zhouquan Liu. Jing Zhang, Junbo Tie, Mingche Lai, Guohui Gong, Gang Chen, Libo Huang.	

Tuesday, September 30 (continued 3 of 3)

	101A	101B	101C	101D
14:50 - 14:55		**Work-in-Progress: MARVEL-PUF: A Robust Multi-Bit Memory PUF for FPGA-based Embedded Systems Security** Atri Chatterjee, Habibur Rahman, Swarup Bhunia		
14:55 - 15:00		**Work-in-Progress: Hermes: An FPGA-based NTT Accelerator Supporting Various Lengths for HHE** Hang Gu, Teng Wang, Qianyu Cheng, Jinao Li, ZhenDong Zheng, Lei Gong, Chao Wang, Xuehai Zhou		
15:00 - 15:30	**Coffee Break & Poster Session**			
15:30 - 17:00	**EMSOFT SS 1:** **Intermittent TinyML: Powering Sustainable Deep Intelligence Without Batteries** Hashan Roshantha Mendis, Kasim Sinan Yildirim, Marco Zimmerling, Luca Mottola, Pi-Cheng Hsiu **Efficient and Sustainable Deep Inference on Intermittent Battery-less Tiny Devices** **Algorithms and Architectures for Intermittent Inference on Battery-less Sensors** **Methods and Tools for Batteryless Intermittent Networks** **Building Up to Intermittent Inference in Space**	**CODES+ISSS SS 1:** **Hardware-Software Co-Design for Machine Learning Systems Made Open-Source** Mehdi Tahoori, Vincent Meyers, Mahboobe Sadeghipour Roodsari, Huashuangyang Xu, Juergen Becker, Felix Frombach, Tanja Harbaum, Julian Hoefer, Georgios Sotiropoulos, Jorg Henkel, Zeynep Demirdag, Heba Khdr, Hassan Nassar, Ulf Schlichtmann, Philipp van Kempen, Johannes Geier, Georg Sigl, Stefan Koegler, Matthias Probst, Jurgen Teich, Frank Hannig, Muhammad Sabih, Batuhan Sesli, Norbert Wehn, Lukas Steiner, Wolfgang Kunz, Mohamed Shelkamy Ali **Accelerator IP Development and Safety Extensions in Open-Source AI Hardware** **Design Space Exploration of Hardware Architectures and DRAM Interfaces for Optimized AI Systems** **Co-Design of AI Applications: ML Compiler and Accelerator Units**	**CASES SS 1:** **Emerging Scope and Design Challenges for Approximate Computing: Optimizing Accuracy-PPA trade-offs and Beyond** Siva Satyendra Sahoo, Bastien Deveautour, Marcello Traiola, Chongyan Gu, Yun Wu, Aditya Japa, Salim Ullah, Akash Kumar **AI-driven Accuracy-PPA Optimization for Approximate Computing** **Balancing Efficiency and Reliability: the Role of Approximate Computing** **Security-driven Approximate Computing** **Accuracy-driven Approximate Computing**	**EMSOFT SS 2:** **Predictable Timing Behavior in Distributed Cyber-Physical Systems** Jian-Jia Chen, Mario Günzel, Dakshina Dasari, Matthias Becker, Edward A. Lee, Timothy Bourke **Cornerstones in Analytical End-to-End Timing Analysis** **Design Strategies to Meet End-to-End Timing Requirements of Cause-Effect Chains** **Why Determinism Matters in Distributed CPS** **Solving Constraints to Schedule Dataflow Synchronous Programs**
18:00 - 22:00	**Banquet (3F, Ballroom I, Grand Hyatt Taipei)**			

Wednesday, October 1

	201ABC			
08:30 - 09:00	**Best Paper Award Ceremony**			
09:00 - 10:00	**KEYNOTE 3: Mindful AI for Adaptive, Resilient, Cyberphysical Human Systems** Speaker: Prof. Nikil Dutt, UC Irvine — Session Chair: Andy Pimentel			
10:00 - 10:30	**Coffee Break**			
	101A	**101B**	**101C**	**101D**
10:30 - 12:00	**EMSOFT 6:** **Embedded Artificial Intelligence and Machine Learning** Session Chair: Borzoo Bonakdarpour	**CODES+ISSS 6:** **Robust System Design** Session Chairs: Hiroyuki Tomiyama and Gunar Schirner	**CASES 6:** **FPGAs, Low-cost Hardware and Approximate Computing** Session Chair: Heba Khdr	
10:30 - 10:50	**SAPar: A Surrogate-Assisted DNN Partitioner for Efficient Inferences on Edge TPU Pipelines** Binqi Sun, Bohua Zou, Yigong Hu, Tomasz Kloda, Ling Wang, Tarek Abdelzaher, Marco Caccamo	**Efficient Video Redaction at the Edge: Human Motion Tracking for Privacy Protection** Haotian Qiao, Vidya Srinivas, Peter Dinda, Robert Dick	**Timekeepers: ML-Driven SDF Analysis for Power-Wasters Detection in FPGAs** Mohamed Fathy, Hassan Nassar, Mohamed A. Abd El Ghany, Jörg Henkel	
10:50 - 11:10	**TimelyNet: Adaptive Neural Architecture for Autonomous Driving with Dynamic Deadline** Jiale Chen, Duc Van Le, Yuanchun Li, Yunxin Liu, Rui Tan	**SecuPilot: A Security Coprocessor-Integrated Platform for Autonomous UAV Security** Yatharth Agarwal, Vijay Raghunathan	**PRINT-SAFE: PRINTed ultra-low-cost electronic X-Design with Scalable Adaptive Fault Endurance** Priyanjana Pal, Tara Gheshlaghi, Haibin Zhao, Michael Hefenbrock, Michael Beigl, Mehdi B. Tahoori	

continues on next page

Wednesday, October 1 (continued 1 of 3)

	101A	101B	101C	101D
11:10 - 11:30	**Dynamic Layer Routing Defense for Real-Time Embedded Vision** Zimo Ma, Xiangzhong Luo, Qun Song, Rui Tan	**OASIS: Optimized Adaptive System for Intelligent SLAM** Alles Rebel, Bryan Donyanavard, Nikil Dutt	**Late-Breaking: LDQNUR: A Low Delay and Quadruple-Node-Upset-Recovery Latch Design for Embedded Systems in Aerospace Applications.** Aibin Yan, Kunming Fan, Wei Li, Zikang Ma, Tianming Ni, Zhengfeng Huang, Xiaolei Wang, Xiaoqing Wen, Patrick Girard. **Late-Breaking: A 340-µW TinyML Using LUT-Based Reservoir Computing on Low-Cost FPGAs.** Kanta Yoshioka, Hakaru Tamukoh. **Late-Breaking: Beyond BNNs: Design and Acceleration of Sub-Bit Neural Networks using RISC-V Custom Functional Units.** Muhammad Sabih, Hazem, Frank Hannig, Jürgen Teich. **Late-Breaking: EMGAxO: Extending Machine Learning Hardware Generators with Approximate Operators.** Ali Asghar, Shahzad Bangash, Suleman Shah, Laiq Hasan, Salim Ullah, Siva Satyendra Sahoo, Akash Kumar.	
11:30 - 11:50	**Star-set based efficient reachable set computation of anytime sensing-based neural network-controlled dynamical systems** Lipsy Gupta, Pavithra Prabhakar	**Developing Deadlock-Free Routing Algorithms in Torus NoC: A Formal Approach** Surajit Das, Abhijit Das, Chandan Karfa		
11:50 - 11:55	**Late-Breaking: Synthesizing Barrier Certificates for Neural Network Controlled Continuous Systems with Uncertain Measurements,** Yi Luo, Xin Chen, Jin Dai, Enyi Tang, Xuandong Li	**Late-Breaking: Instruction-Level Support for Deterministic Dataflow in Real-Time Systems** Bo Zhang, YinKang Gao, Caixu Zhao, Chao Wang, Xi Li		

Wednesday, October 1 (continued 2 of 3)

	101A	101B	101C	101D
11:55 - 12:00	**Work-in-Progress: Enabling Skew-aware Federated Learning on Embedded Systems via Non-IID Data Distribution Type Estimation,** Tatsuya Nishio, Hiroki NIshikawa, Ittetsu Taniguchi, Takao Onoye	**Late-Breaking: Minimizing Backbone Ethernet Traffic for Enabling Inter-zonal Messages in Software-Defined Vehicles** Ashiqur Rahaman Molla, Ram Mohan Chowdary Kota, Jaishree Mayank, Arnab Sarkar, Arijit Mondal, Soumyajit Dey		
12:00 - 12:30	**Poster Session**			
12:30 - 13:30	**Lunch Break (4F VIP Room)**			**PhD Forum & Recruitment (Lunch)**
13:30 - 15:00	**EMSOFT 7: Under the hood** Chair: Björn Brandenburg	**CODES+ISSS 7: Application-Specific Optimizations** Session Chairs: Jenq-Kuen Lee and Bryan Donyanavard	**CASES SS 2: Design and Optimization for AI/ML Acceleration on Resource-constrained Systems** Jalil Boukhobza, Alessio Burrello, Yuan-Hao Chang, Yawei Li, Daniele Jahier Pagliari, Chun-Feng Wu, Ming-Chang Yang, Tsun-Yu Yang	
13:30 - 13:50	**App-Aware Swap Resource Allocation for Enhancing User-Perceived Latency on Mobile Devices** Yi-Cheng Wei, Yi-Chieh Tsou, Yong-Cheng Chen, Li-Pin Chang	**Unlocking the Full Potential of Dual-Interface SSDs: A Comprehensive Hardware and Software Perspective** Lok Yin Chow, Yingjia Wang, Yuhong Liang, Ming-Chang Yang		
13:50 - 14:10	**LazyTick: Lazy and Efficient Management of Job Release in Real-Time Operating Systems** Kay Heider, Christian Hakert, Kuan-Hsun Chen, Jian-Jia Chen	**Work-in-Progress: Extending a RISC-V Core with Sub-FP8 Support for Machine Learning** Kathryn Julia Chapman, Fu-Jian Shen, Jhih-Kuan Lin, Jenq-Kuen Lee **Work-in-Progress: SIMD-CP: SIMD with Redundant Bits Compression and Mixed-Precision Packing for Quantized DNNs** Hayata Kaneko, Lin Meng **Late-Breaking: Towards Efficient FPGA Accelerator DSE via Hierarchical and RM-Guided Methods** Chao Shi, Qianyu Cheng, Teng Wang, Chao Wang, Xuehai Zhou **Work-in-Progress: MIVAS: Adaptive Residual Value Mining in Self-Powered Systems from the Scheduling Perspective** Xuejin Li, Keni Qiu	**Hardware-aware DNN Architecture and Mapping Co-optimization for Efficient Inference on Resource-constrained Heterogeneous Systems** **Scaling RAG on Resource-constrained Systems: Advanced Memory, Storage, and Energy-efficient Designs for Next-Gen AI** **Towards Cost-effective and High-performance Large-Scale Graph Processing on Resource-constrained Systems** **Learning on the Edge: Unlocking the Storage Bottleneck with a Divide and Conquer Approach for Resource-constrained Edge Systems**	

Wednesday, October 1 (continued 3 of 3)

	101A	101B	101C	101D
14:10 - 14:30	**Ember: Task Wakeup Sequence Based Energy Optimization for Mobile Web Browsing** Seonghoon Park, Jiwon Kim, Jeho Lee, Hojung Cha	**Work-in-Progress: Softtide: a deterministic middleware for real-time systems** Jiajie Wang, Saumya Shankar, Partha Roop **Work-in-Progress: Dual-Mode Rounding Algorithms and Hardware for Posit-based DNN Training: The Future of Mixed Precision Frameworks** Vishesh Mishra, Mahendra Rathor, Urbi Chatterjee **Work-in-Progress: JDFuzz: A Hardware-Software Approach for Accelerating Fuzzing Embedded Systems** Weiye He, Junyan Ma		
14:30 - 14:50	**Wasm-IO: Enabling Low-Level Device Interaction in WebAssembly for Industry Automation** Maximilian Seidler, Alexander Krause, Peter Ulbrich			
14:50 - 14:55	**Late-Breaking: Container-based Fail-operational System Architecture for Software Defined Vehicles,** Changjo Cho, Hamin An, Jangho Shin, Jong-Chan Kim			
14:55 - 15:00				
15:00 - 15:30	**Coffee Break & Poster Session**			
	201ABC			
15:30 - 17:00	**PANEL**			
17:00 - 17:30	**Closing Session**			

ESWEEK 2025 SCHEDULE AT-A-GLANCE

Thursday, October 2

	101A	101B	101C	101D
09:00 - 10:30	**MEMOCODE (Opening Remarks and Keynote)**		**TCRS (Opening Remarks and Keynote)**	**MSC (Opening remarks and Keynote)**
9:00 - 9:15	**Opening Remarks** by Prof. Nan Guan, City University of Hong Kong	**Opening Remarks** by Prof. Georgiy Krylov, University of New Brunswick	**Opening Remarks** by Prof. Hokeun Kim, Arizona State University	**Opening Remarks** by Prof. Ya-Shu Chen, National Taiwan University of Science and Technology
9:20 - 10:30	**Keynote Distributed computing on bittide systems** Speaker: Prof. Sanjay Lall, Stanford University		**Keynote Time Sensitive Requirement and Applications for Connected Vehicles** Speaker: Prof. Chi-Sheng Shih, National Taiwan University	**Keynote A Decade of Research on Hybrid Cloud Storage Systems: A Retrospective** Speaker: Prof. Jalil Boukhobza, ENSTA
10:30 - 11:00	**Coffee Break**			
11:00 - 12:30	**MEMOCODE - Regular Session 1** (Contract based design/ reasoning) Session Chair: Pierluigi Nuzzo	**RSP - Session 1** (Networking, SoCs, and Autonomous Systems) Session Chair: Kenneth Kent	**TCRS - Session 1** (Real-Time Coordination for Connected and Intelligent Vehicles) Session Chair: Jeronimo Castrillon	**MSC -Session 1** (Performance and Reliability Issues of Processing/ Logic-in-Memory) Session Chair: Che-Wei Chang
11:00 - 11:30	**Contract-based Component Selection Using Behaviors,** Sheng-Jung Yu, Alberto Sangiovanni-Vincentelli	**A Prototyping Framework for P4-Programmable Traffic Managers,** Karl La Grassa, André Beliveau, Mathieu Leonardon, Jean-Pierre David, Matthieu Arzel, Yvon Savaria **Dynamic Asynchronous Controller for Integrated Photonic Networks: Introducing CLAP,** Felipe Gohring De Magalhaes **CART: Combined AUTOSAR AP and ROS 2 Tracing Framework,** Ryudai Iwakami, Hiroyukia Hanyu, Tasuku Ishigooka, Takuya Azumi **RISC-B: Hardware Blocks for the design of RISC-V-based SoCs,** Carlos Andres Lara-Nino	**Value-Aware Real-Time Scheduling for Intelligent Transportation Systems,** Hoeseok Yang, Hokeun Kim, Choonghwan Lee, Hyung-Chan An	**Scalable Cross-layer Reliability Evaluation in Bulk-Bitwise Logic-in-Memory,** João Paulo Cardoso de Lima
11:30 - 12:00	**Ensuring Strong Replaceability of Assume-guarantee Contract for Feedback Composition,** Sheng-Jung Yu, Alberto Sangiovanni-Vincentelli		**Software-Defined Vehicles: Challenges and Orchestrating Mixed-Criticality Services Using Lingua Franca,** Wenhung Kevin Huang, Yoshinori Terazawa, Yutaka Matsubara, Akihito Iwai	**Enabling Edge Intelligence with ReRAM-based Processing-in-Memory Architectures,** Chin-Fu Nien
12:00 - 12:30	**Work-in-Progress:Formal Analysis of Fault Propagation in Complex Digital Systems,** Damiano Zuccala, Mohammad Reza Heidari Iman, Katell Morin-Allory, Samuel Hon, Jean-Marc Daveau, Philippe Roche		**Compatibility Analysis and Smooth Transition of Heterogeneous Controllers in Longitudinal Merging Platoons,** Pintusorn Suttiponpisarn, Chung-Wei Lin	**Harnessing Processing-in-Memory to Mitigate Data Movement in Memory-Intensive Workloads,** Chien-Chung Ho
12:30 - 13:30	**Lunch Break (4F Joy Lounge)**			

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Thursday, October 2 (continued 1 of 2)

	101A	101B	101C	101D
13:30 - 15:00	**MEMOCODE- Regular Session 2** (Timed systems, Task graph modeling,...) Session Chair: Benjamin Lion	**RSP -Session 2** (Hardware Platforms and Energy Efficiency) Session Chair: Felipe Gohring De Magalhaes	**TCRS -Session 2** (System and Architecture Design for Time-Sensitive Software) Session Chair: Chung-Wei Lin	**MSC -Session 2** (Key Storage Technologies in Future AI Systems and Applications) Session Chair: Po-Chun Huang
13:30- 14:00	**Optimal Real-time Inter-zone Message Communication via Ethernet Backbone in Software Defined Vehicles,** Ram Mohan Chowdary Kota, Ashiqur Rahaman Molla, Jaishree Mayank, Arnab Sarkar, Arijit Mondal, Soumyajit Dey	**ADAM: ADAptive Microcontroller Platform for Edge AI Systems,** Felipe Paiva Alencar, Aymen Romdhane, Bruno Lovison Franco, Yann Guilhot, Jonathan Miquel, Théo Soriano, David Novo, Pascal Benoit **Exploring Cache Policies on FPGA-Accelerated Simulations: Tradeoffs Between Usability and Simulation Speed,** Soraya Mobaraki, Gil Thierry, Lionel Torres, David Novo **From Concept to FPGA Prototype: System Design and Verification for the Control of 3-Phase PMSM,** Maxime Gras-Chevalier, Christophe Jégo, Camille Leroux, Franck Guillemard **Lightweight UNet-1D-CPCA Regression Model for Energy-Efficient Blood Pressure Estimation from Raw PPG Signals,** Amir Arjomand, Kenneth B. Kent, Georgiy Krylov	**Deterministic Modeling and Simulation of Fault-Tolerant Real-Time Software,** Dongha Kim, Hokeun Kim	**From Bottleneck to Breakthrough: CXL Memory Expansion for AI Workstations,** Yu-Ming Chang
14:00 - 14:30	**Coherence-Aware Task Graph Modeling for Realistic Application,** Guochu Xiong, Xiangzhong Luo, Weichen Liu		**ForSyDe on the Patmos Processor,** Ehsan Khodadad, Ingo Sander, Luca Pezzarossa, Martin Schoeberl	**Analysis and Optimized CXL-Attached Memory Allocation for Long-Context LLM Fine-Tuning,** Shou-Han Chen
14:30 - 15:00	**Work-in-Progress: Optimising the Scheduling of System Level Logical Execution Time Systems,** Jamie Lee, Nathan Allen, Matthew M. Y. Kuo, Eugene Yip		**LLVM-Based Hybrid Cache and TCM Memory Allocation Optimization for Low-Latency, Energy-Efficient Execution,** Gihyeon Jeon, Daejin Park	**Distilling Flash Blocks to Unify Flash Pages of a Superpage in an SSD,** Tseng-Yi Chen
15:00 - 15:30	**Coffee Break**			

Thursday, October 2 (continued 2 of 2)

	101A	101B	101C	101D
15:30 - 17:00	**MEMOCODE- Regular Session 3 (Learning based systems)** Session Chair: Joao Paulo Cardoso de Lima	**RSP -Session 3 (Compiler and Simulation Innovations)** Session Chair: Frédéric Rousseau	**TCRS -Session 3 (Towards Timely and Safe Neural Networks)** Session Chair: Hoseok Yang	
15:30- 16:00	**Compositional training for Safe AI-based Cyber-Physical Systems,** Sobhan Chatterjee, Saumya Shankar, Partha Roop	**Control-flow aware MLIR tracing,** Gaëtan Lounes, Robin Gerzaguet, Matthieu Gautier **Early Detection of Unsupported Compilations during Prototyping in a Template-based Just-in-Time Compiler,** Michael Goodyear, Scott Young, Marius Pirvu, Harpreet Kaur, Kenneth Kent **Extending Instruction Set Simulators with ML-based Performance Models: Application to QEMU,** Igor Macanovic, Fatma Jebali and Caaliph Andriamisaina **Evaluation Tool for Stencil Application Memory Usage,** Kilian McGovern, Fédéric Rousseau, Henri-Pierre Charles	**Combining Early Exit and Selective Prediction for Convolutional Neural Networks,** Hasna Bouraoui, Chadlia Jerad, Jeronimo Castrillon	
16:00 - 16:30	**Work-in-Progress: Hyperproperty-Constrained Secure Reinforcement Learning,** Ernest Bonnah, Luan Nguyen, Khaza Anuarul Hoque		**Safety-Driven DNN Sizing for Vehicular CPS,** Tingan Zhu, Mier Li, Bineet Ghosh, Samarjit Chakraborty, Parasara Sridhar Duggirala	
16:30 - 17:00	**Interaction/Discussion**			

Friday, October 3

	101A
09:00 - 10:30	**MEMOCODE (Keynote)**
09:00 - 10:15	**Keynote** **Formal Design of Safety-critical Embedded Systems** Speaker: Prof. Naijun Zhan, Peking University Session Chair: Partha Roop
10:30 - 11:00	**Coffee Break**
11:00 - 12:30	**MEMOCODE Regular Session 4** **(Invited Papers)** Session Chair: Sanjiva Prasad
11:00 - 11:30	**Formal Methods for Cryogenic Cyber Physical Systems (CCPS),** Duleepa Thrimawithana, Partha Roop, Sobhan Chatterjee, Maryam Hemmati
11:30 - 12:00	**Time Aware Compilation Verified: A Category-Theoretic Approach in Rocq,** Benjamin Lion, David Nowak
12:00 - 12:30	**Tuning into my heart through wearables: Towards a novel formal cardiac digital twin,** Partha Roop, Nathan Allen, Shahab Kazemi
12:30 - 13:30	**Lunch Break (4F Joy Lounge)**
13:30 - 15:00	**MEMOCODE Regular Session 5** **(Embedded and CPS, Security)** Session Chair: Chia-Yin Liu
13:30- 14:00	**Mitigation of Cyber-physical Attacks in Industry 4.0 using Secure Function Blocks,** Steph Wu, Alex Baird, Partha Roop, Nathan Allen, Hammond Pearce
14:00 - 14:20	**Work-in-Progress: Efficient compilation and execution of synchronous programs via type-state programming,** Avinash Malik
14:20 - 14:40	**Work-in-Progress: Automated Power Domain Insertion and Control in Dataflow Circuits,** Martha Barker, Stephen A. Edwards, Martha Kim, Mark Santolucito
14:40 - 15:00	**Closing remarks** **(Prof. Nan Guan, City University of Hong Kong)**

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